

Alma Correlator Station Card Test Report

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1) Introduction

Initial testing of the ALMA correlator station card prototype was completed in late March 2001 and this report gives results of the tests run. The work done on the prototype station card was in the nature of a preliminary test phase in that the final card test fixture was not ready and, hence, it was not yet possible to test the card completely. Instead, an old GBT spectrometer test fixture was modified and used to drive the microprocessor port of the card to be tested.

With the microprocessor port on this test fixture, the personalities for the card FPGA chips could be downloaded and various tests performed. All of the tests run pertained to internal card functions (microprocessor port functions, card RAM functionality, card high-speed signal runs, or functions internal to individual FPGA chips). Without the test fixture, no card interface signals except the microprocessor port could be evaluated (that is, the normal card input signals were not supplied with input drive and the drive from normal card output signals were not tested in any way). Otherwise, the report below describes the tests run.

2) Test Summary

The initial testing of the station card went as smoothly as could be expected. No card layout or logic errors were encountered as testing of the card progressed. The final step in the card test involved verifying the integrity and speed of data paths through the card RAM buffers. During this part of the card test, two RAM chip pins were found to be unsoldered and these faults remain the only problems found.

3) FPGA and CPLD Description

Most of the logic functions on the ALMA correlator station card are performed in programmable logic chips and interstage RAM buffers. There is one CPLD and 3 FPGA designs:

- CPLD microprocessor interface port
- Input DEMUX FPGA design (splits 32 input data lines into 64 for drive into the RAM buffers)
- ADDRESS FPGA design (generates complex RAM address sequences required for data re-blocking)
- Output MUX FPGA design (re-combines 64 parallel RAM outputs to 32 data packet card outputs)

The table below gives statistics on the station card CPLD and FPGA designs. The utilization column indicates the percentage of internal logic cells available in the part that are actually used. The Max clock rate column is a worst case estimate of part speed made by the Xilinx Foundations software package based on the actual design routing.

Design	Part	Utilization	# F/F	IO pins used	Max clock rate
Interface	XC95144XL-10	57%	33	65	-
DEMUX	XCV50E-6	70%	871	149	139 MHz
ADDRESS	XCV200E-6	83%	1798	143	145 MHz
MUX	XCV100E-6	88%	1968	145	138 MHz

4) Power Considerations

With the card loaded with operational FPGA personalities, the power requirements for the card could be measured using as card inputs pseudo random data being generated in the DEMUX FPGA chips. The table

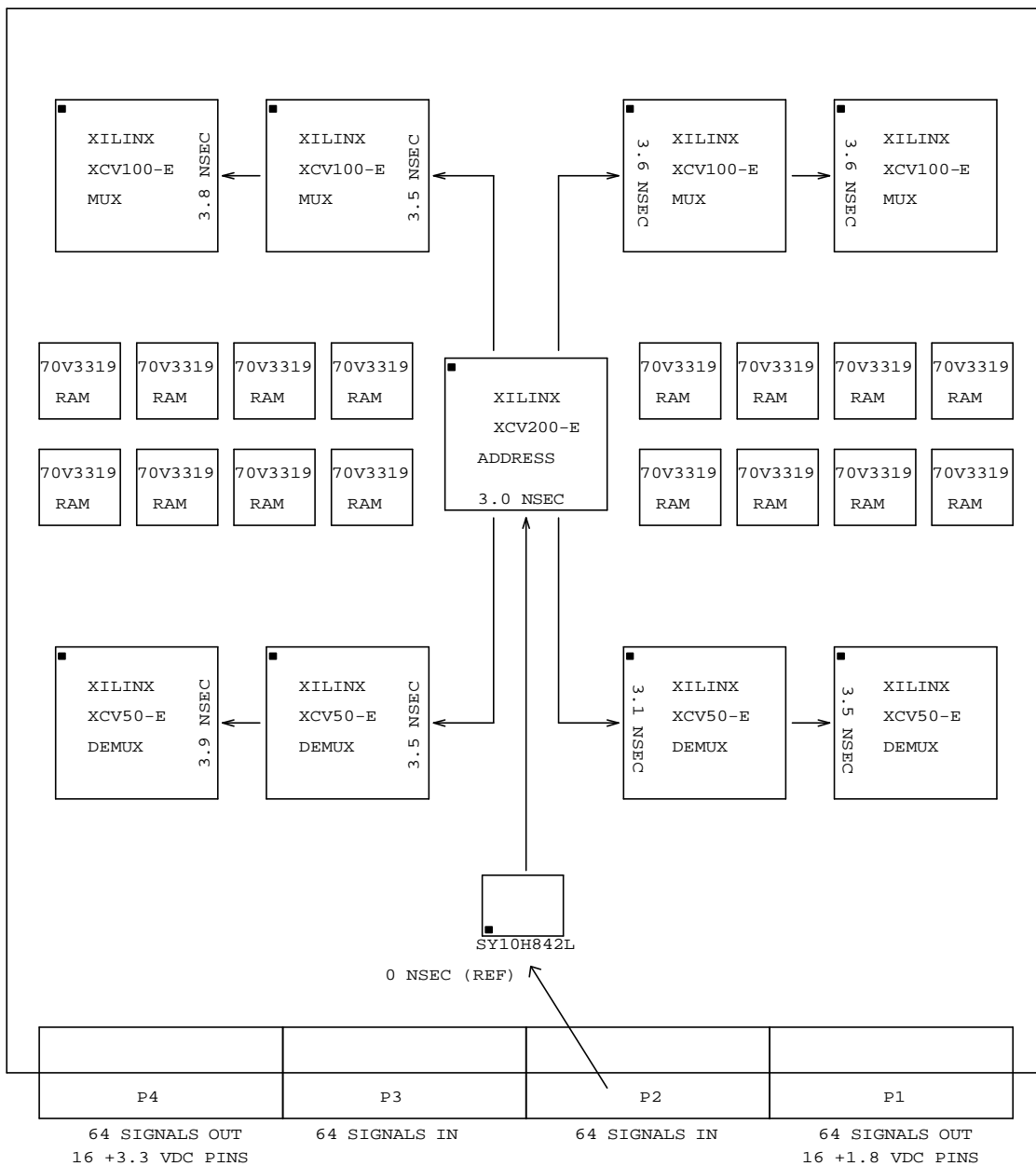
below gives the results of the power measurements made on the 1.8 VDC and 3.3 VDC power supplies

- 3.3 VDC supply current requirement was 4.11 amps
- 1.8 VDC supply current requirement was 3.52 amps
- total card power dissipation was thus about 20 watts

5) Clock skew

The method of clock distribution adopted for the ALMA correlator is: drive the card with a single sinewave clock at the 125 MHz system clock rate, square to logic levels using a Synergy SY10H842 IC whose output supplies clock to one or two Virtex FPGA chips, and use the zero propagation delay feature of the Virtex delay lock loop (DLL) to daisy chain FPGA chips. The figure below illustrates clock distribution on the station card (all FPGA clock drive signals had slew rate set to FAST and drive level set to 12 ma):

STATION CARD



The times seen in the figure above gives the clock timing as measured on the station card using in input pin of the SY10H842L chip as the reference (0 nsec).

6) Card Tests

A number of tests to checkout various parts of the station card were programmed in assembly language on the GBT test fixture Dallas 87C520 microprocessor.

In testing high speed (125 MHz clock rate) chip-to-chip data quality, 35-bit pseudo random data generators in the FPGAs were used as the signal source (yielding about a 4.5 second pattern repeat duration). The data error rate was measured at the receive end of a data path by loading 35 consecutive bits of receive data into a duplicate 35-bit data generator (that is, using 35 bits of input data as a seed for a predict pseudo random data generator).

Once loaded with bits from the path to be tested, the predict generator feedback path was closed and the resulting pattern compared to subsequent bits from the data signal being tested. An error count was made for 1 millisecond and then read by the 87C520 microprocessor.

Below is a description of tests run on the prototype station card:

TEST0 through TEST4

Tests 0 through 4 were tests of the card input microprocessor port and the on-card CPLD-to-FPGA communication links. In each test, pseudo random data from the 87C520 microprocessor was written to various targets on the station card and then read back to verify error free operation in both directions.

The card CPLD has two 8-bit registers that can be written to and read on the microprocessor port. TEST0 loops testing these two registers. The DEMUX FPGA chips have a 4-byte register that was tested by using TEST1. TEST2 tested a 2-byte register in the ADDRESS FPGA design and TEST3 tested 4-byte register in the MUX chips. TEST4 was a combination of TEST0 through TEST3.

All of the tests ran error free.

TEST5, TEST6, and TEST7

Tests 5, 6, and 7 wrote 256 or 512 byte pseudo random data arrays into block RAMs internal to the FPGA chips and then read them to test for error free operation. There is a single 256-byte RAM in the DEMUX chip design (tested in TEST5), six 256-byte RAMs in the ADDRESS design (tested in TEST6), and eight 512-byte RAMs in the MUX design (tested in TEST7).

Tests 5, 6, and 7 all ran error free.

TEST8 and TEST9

There are 16-bit (125 MHz clock rate) data transfers between pairs of DEMUX chips and also between pairs of MUX chips on the station card. TEST8 tested the DEMUX-to-DEMUX interfaces and TEST9 the MUX-to-MUX interfaces.

Both TEST8 and TEST9 used 35-bit pseudo random data generators in one FPGA chip to drive the opposite chip where the data quality test was performed. The card clock rate was varied over a range from 100 MHz to 158 MHz in order to test the card speed performance margin.

All runs of TEST8 and TEST9 resulted in error free operation to at least 155 MHz.

TESTA

TESTA was the most comprehensive test run on the station card. This test was the only test to include the station card main RAM buffers (there are four 64K X 64 buffers on the station card requiring a total of 16 RAM chips).

In TESTA, the DEMUX chip 35-bit data generators were used as the signal source. The test patterns generated at the input to the DEMUX chips were processed the normal way in the DEMUX chips, written into the card RAM buffers, and finally read in 1-millisecond data packets from the RAM buffers by the MUX chips as in normal operation.

TESTA resulted in error free operation up to a card clock rate of a little over 150 MHz.