



LOC=P1 IOPAD \$I209 IN0
 LOC=P2 IOPAD \$I210 IN1
 LOC=P3 IOPAD \$I211 IN2
 LOC=P4 IOPAD \$I212 IN3
 LOC=P6 IOPAD \$I213 IN4
 LOC=P7 IOPAD \$I214 IN5
 LOC=P8 IOPAD \$I215 IN6
 LOC=P9 IOPAD \$I216 IN7

LOC=P10 IPAD \$I233 CTRL-0 \$I234 CTRL0
 LOC=P11 IPAD \$I235 CTRL-1 \$I236 CTRL1
 LOC=P12 IPAD \$I237 CTRL-2 \$I238 CTRL2
 LOC=P13 IPAD \$I239 CTRL-3 \$I240 CTRL3
 LOC=P14 IPAD \$I241 CLK-IN \$I242 CLK

CTRLx [X][X][X][X]
 CLK [X]

CTRL0 A0 D0 SEL0
 CTRL1 A1 D1 SEL1
 CTRL2 A2 D2 SEL2
 CTRL3 A3 D3 SEL3
 CTRL3 A4 D4 SEL4
 CTRL3 A5 D5 SEL5
 CTRL3 A6 D6 SEL6
 CTRL3 A7 D7 SEL7

CTRL0 A0 D0 SEL8
 CTRL1 A1 D1 SEL9
 CTRL2 A2 D2 SEL10
 CTRL3 A3 D3 SEL11
 CTRL3 A4 D4 SEL12
 CTRL3 A5 D5 SEL13
 CTRL3 A6 D6 SEL14
 CTRL3 A7 D7 SEL15

D[7:0] D[7:0] S[7:0]
 SEL0 CE \$I325 CONTROL REGISTER
 CLK C CLR
 LOW

D[7:0] D[7:0] TP-SEL[7:0]
 SEL3 CE \$I386 TEST POINT SELECT REGISTER
 CLK C CLR
 LOW

FUNCTION	CTRL[3:0]	SELECT
WRITE TO CPLD CONTROL REGISTER	0 0 0 0	SEL0
WRITE TO CPLD BROADCAST REGISTER 1	0 0 0 1	SEL1
WRITE TO CPLD BROADCAST REGISTER 2	0 0 1 0	SEL2
WRITE TO CPLD TEST POINT SELECT REG	0 0 1 1	SEL3
WRITE TO FPGA CONTROL REGISTER	0 1 0 0	SEL4
BROADCAST TO FPGA CONTROL REGISTER	0 1 0 1	SEL5
WRITE DATA TO FPGA	0 1 1 0	SEL6
BROADCAST TO FPGA	0 1 1 1	SEL7
READ CPLD MONITOR BYTE	1 0 0 0	SEL8
READ CPLD BROADCAST REGISTER 1	1 0 0 1	SEL9
READ CPLD BROADCAST REGISTER 2	1 0 1 0	SEL10
READ FPGA BYTE	1 0 1 1	SEL11
ONOFF REGISTER	1 1 0 0	SEL12
	1 1 0 1	SEL13
	1 1 1 0	SEL14
	1 1 1 1	SEL15

* PRIMARILY FOR TEST PURPOSES (WRITE/READ TESTS)

MON0 D0 READ0
 BC-SEL0 D1 \$I416
 RET0 D2
 D3
 S0
 S1
 S2
 S3 \$I385

MON1 D0 READ1
 BC-SEL1 D1 \$I420
 RET1 D2
 D3
 S0
 S1
 S2

MON2 D0 READ2
 BC-SEL2 D1 \$I418
 RET2 D2
 D3
 S0
 S1

MON3 D0 READ3
 BC-SEL3 D1 \$I417
 RET3 D2
 D3
 S0
 S1

MON4 D0 READ4
 BC-SEL4 D1 \$I425
 RET4 D2
 D3
 S0
 S1

MON5 D0 READ5
 BC-SEL5 D1 \$I421
 RET5 D2
 D3
 S0
 S1

MON6 D0 READ6
 BC-SEL6 D1 \$I424
 RET6 D2
 D3
 S0
 S1

MON7 D0 READ7
 BC-SEL7 D1 \$I419
 RET7 D2
 D3
 S0
 S1

SEL9 \$I422
 SEL11 \$I423

MON0 D0
 BC-SEL0 D1
 RET0 D2
 D3
 S0
 S1
 S2
 S3

MON1 D0
 BC-SEL1 D1
 RET1 D2
 D3
 S0
 S1
 S2

MON2 D0
 BC-SEL2 D1
 RET2 D2
 D3
 S0
 S1

MON3 D0
 BC-SEL3 D1
 RET3 D2
 D3
 S0
 S1

MON4 D0
 BC-SEL4 D1
 RET4 D2
 D3
 S0
 S1

MON5 D0
 BC-SEL5 D1
 RET5 D2
 D3
 S0
 S1

MON6 D0
 BC-SEL6 D1
 RET6 D2
 D3
 S0
 S1

MON7 D0
 BC-SEL7 D1
 RET7 D2
 D3
 S0
 S1

SEL9 \$I422
 SEL11 \$I423

MON0 D0
 BC-SEL0 D1
 RET0 D2
 D3
 S0
 S1
 S2
 S3

MON1 D0
 BC-SEL1 D1
 RET1 D2
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MON2 D0
 BC-SEL2 D1
 RET2 D2
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MON3 D0
 BC-SEL3 D1
 RET3 D2
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MON4 D0
 BC-SEL4 D1
 RET4 D2
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MON5 D0
 BC-SEL5 D1
 RET5 D2
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MON6 D0
 BC-SEL6 D1
 RET6 D2
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MON7 D0
 BC-SEL7 D1
 RET7 D2
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 S0
 S1

SEL9 \$I422
 SEL11 \$I423

MON0 D0
 BC-SEL0 D1
 RET0 D2
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MON1 D0
 BC-SEL1 D1
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MON2 D0
 BC-SEL2 D1
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MON3 D0
 BC-SEL3 D1
 RET3 D2
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MON4 D0
 BC-SEL4 D1
 RET4 D2
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MON5 D0
 BC-SEL5 D1
 RET5 D2
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 S0
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MON6 D0
 BC-SEL6 D1
 RET6 D2
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MON7 D0
 BC-SEL7 D1
 RET7 D2
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SEL9 \$I422
 SEL11 \$I423

MON0 D0
 BC-SEL0 D1
 RET0 D2
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MON1 D0
 BC-SEL1 D1
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MON2 D0
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MON3 D0
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MON4 D0
 BC-SEL4 D1
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MON5 D0
 BC-SEL5 D1
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MON6 D0
 BC-SEL6 D1
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MON7 D0
 BC-SEL7 D1
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SEL9 \$I422
 SEL11 \$I423

MON0 D0
 BC-SEL0 D1
 RET0 D2
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MON1 D0
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MON2 D0
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MON3 D0
 BC-SEL3 D1
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MON4 D0
 BC-SEL4 D1
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MON5 D0
 BC-SEL5 D1
 RET5 D2
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MON6 D0
 BC-SEL6 D1
 RET6 D2
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MON7 D0
 BC-SEL7 D1
 RET7 D2
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 S0
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SEL9 \$I422
 SEL11 \$I423

MON0 D0
 BC-SEL0 D1
 RET0 D2
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MON1 D0
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MON2 D0
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MON3 D0
 BC-SEL3 D1
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MON4 D0
 BC-SEL4 D1
 RET4 D2
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MON5 D0
 BC-SEL5 D1
 RET5 D2
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MON6 D0
 BC-SEL6 D1
 RET6 D2
 D3
 S0
 S1

MON7 D0
 BC-SEL7 D1
 RET7 D2
 D3
 S0
 S1

SEL9 \$I422
 SEL11 \$I423

CONFIGURATION:
 S0 = 0
 OPERATION:
 S0 = 1

SEL4
 SEL5
 SEL6
 SEL7

SC-SEL = SINGLE CLOCK SELECT
 BC-SEL = BROADCAST CLOCK SELECT

S0 = 0 TO LOAD XILINX PERSONALITY

GLITCH AT FALLING EDGE OF S0 SHOULD NOT BE A PROBLEM

S0 = 0 TO LOAD XILINX PERSONALITY
 S1 PULSED HIGH TO INITIATE LOAD XILINX PERSONALITY

DURING CONFIGURATION, THESE ARE CHIP SELECTS
 DURING OPERATION, THEY ARE CLOCKS

PROG# \$I272
 CCLK0 \$I275
 CCLK1 \$I277
 CCLK2 \$I278
 CCLK3 \$I281
 CCLK4 \$I258
 CCLK5 \$I258

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