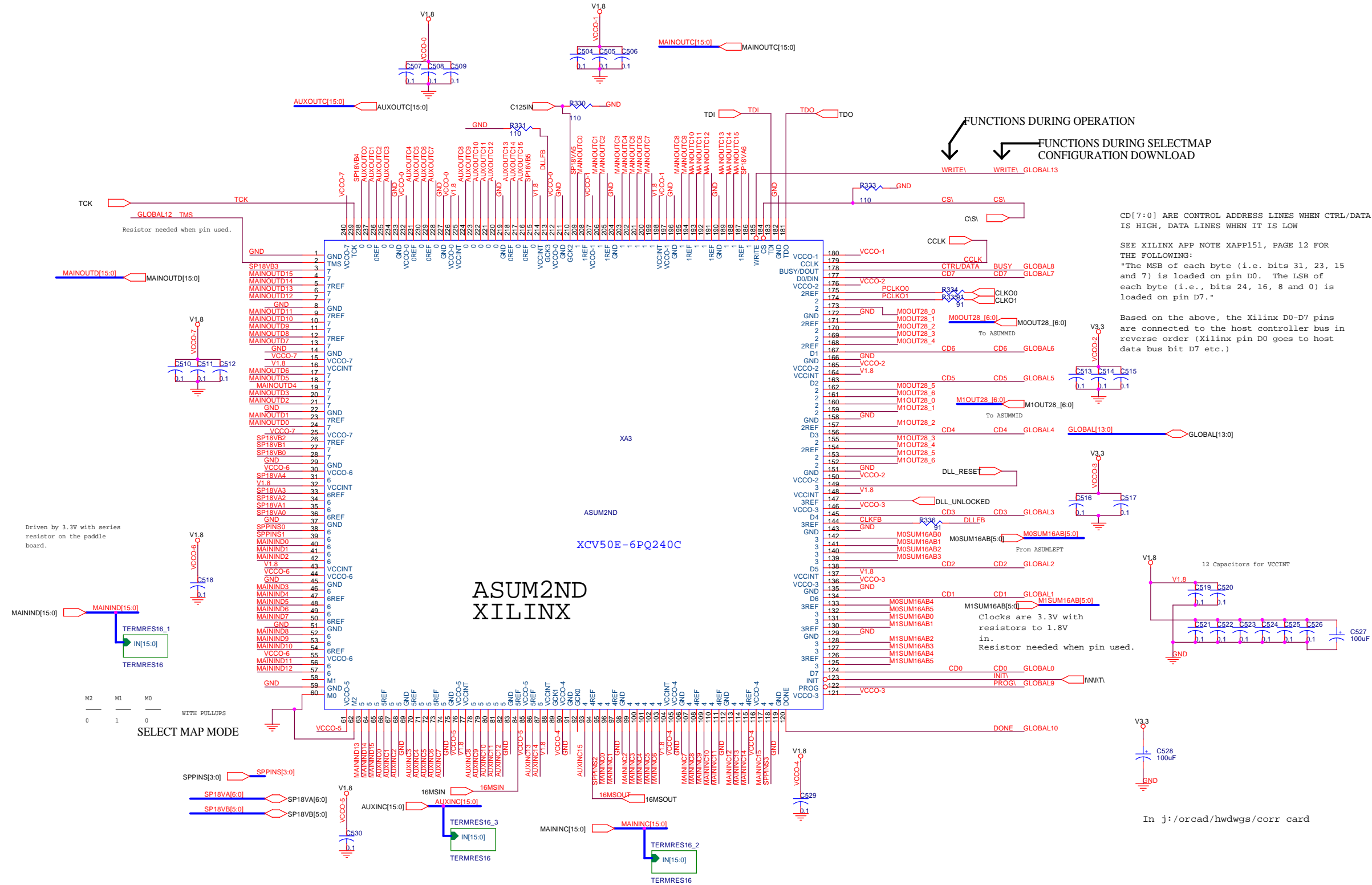


Edit part, then select the pins and edit properties to change to inputs or outputs.

MIRROR IMAGED SINCE ON BACK OF CARD  
MAIND0 MAIND15 AUXC0 AUXC15 MAINC0 MAINC15



CD[7:0] ARE CONTROL ADDRESS LINES WHEN CTRL/DATA IS HIGH, DATA LINES WHEN IT IS LOW

SEE XILINX APP NOTE XAPP151, PAGE 12 FOR THE FOLLOWING:  
"The MSB of each byte (i.e. bits 31, 23, 15 and 7) is loaded on pin D0. The LSB of each byte (i.e., bits 24, 16, 8 and 0) is loaded on pin D7."

Based on the above, the Xilinx D0-D7 pins are connected to the host controller bus in reverse order (Xilinx pin D0 goes to host data bus bit D7 etc.)

ASUM2ND  
XILINX

**XILINX VIRTEX-E XCV50E-6PQ240C FPGA**

MAIND0 MAIND15 AUXC0 AUXC15 MAINC0 MAINC15

In j:\orcad\hwdwgs\corr card

Title		ALMA Correlator Board	
Size	C	Document Number	08060200s001
Date:	Friday, May 25, 2001	Sheet	72 of 133