

Edit part, then select the pins and edit properties to change to inputs or outputs.

Output bus from 4 asics. From LTA with resistor termination. Or from other Xilinx.

Left and Right swapped since on back of card.

To Dataout Xilinx on the right, viewed from top.

Spare 3.3V pins

Resistor needed when pin used.

Intersection and block address to ASICs in parallel

Powered by V1.8.

External 74lvc139a to provide Asic OEs.

WITH PULLUPS

SELECT MAP MODE

Output bus from 4 asics.

From above Dataout Xilinx.

FUNCTIONS DURING OPERATION

FUNCTIONS DURING SELECTMAP CONFIGURATION DOWNLOAD

CD[7:0] ARE CONTROL ADDRESS LINES WHEN CTRL/DATA IS HIGH, DATA LINES WHEN IT IS LOW

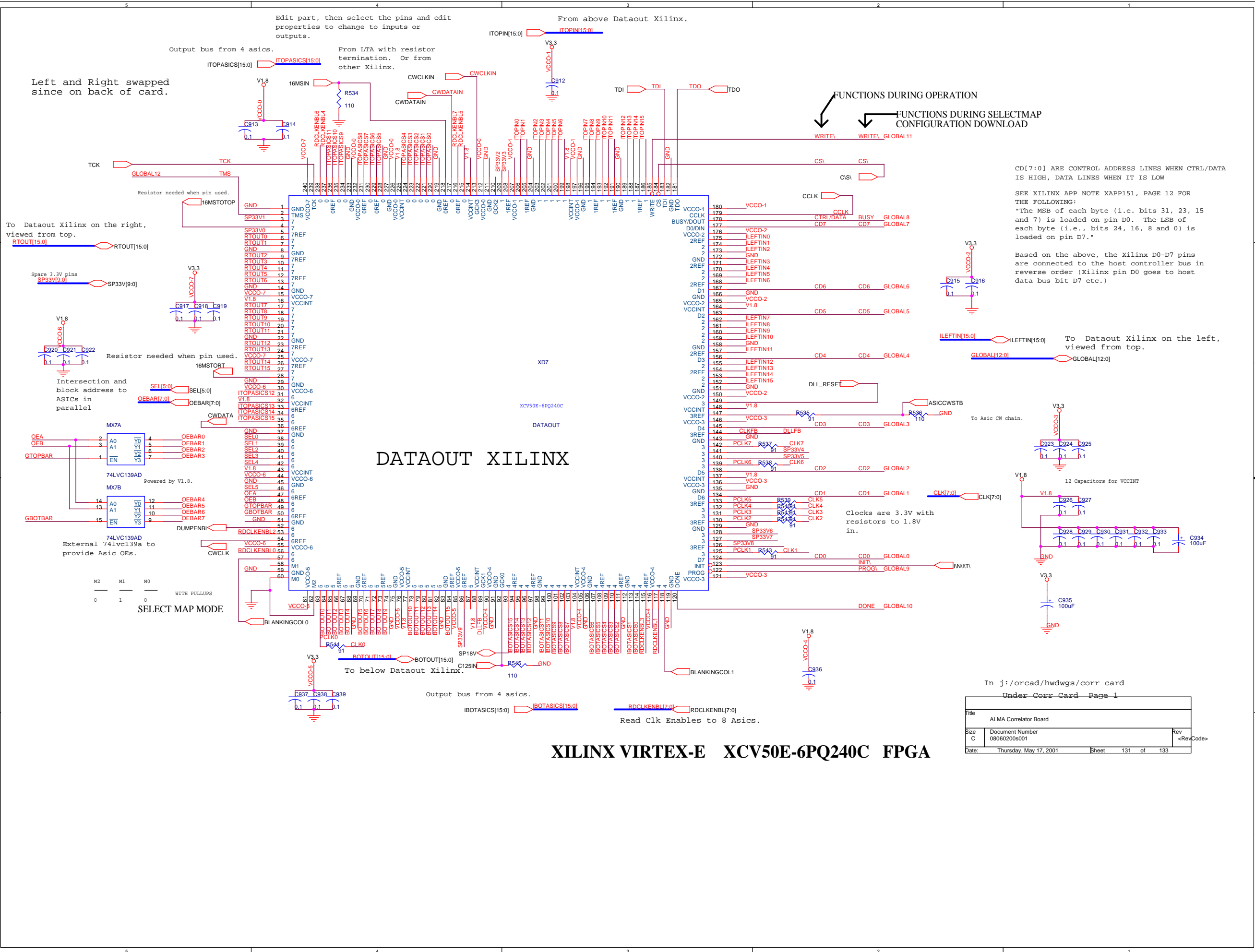
SEE XILINX APP NOTE XAPP151, PAGE 12 FOR THE FOLLOWING:
"The MSB of each byte (i.e. bits 31, 23, 15 and 7) is loaded on pin D0. The LSB of each byte (i.e., bits 24, 16, 8 and 0) is loaded on pin D7."

Based on the above, the Xilinx D0-D7 pins are connected to the host controller bus in reverse order (Xilinx pin D0 goes to host data bus bit D7 etc.)

To Dataout Xilinx on the left, viewed from top.

DATAOUT XILINX

XILINX VIRTEX-E XCV50E-6PQ240C FPGA



In j:\orcad\hwdwgs\corr card
Under Corr Card Page 1

Title ALMA Correlator Board		
Size C	Document Number 08060200s001	Rev <RevCode>
Date: Thursday, May 17, 2001	Sheet 131 of 133	