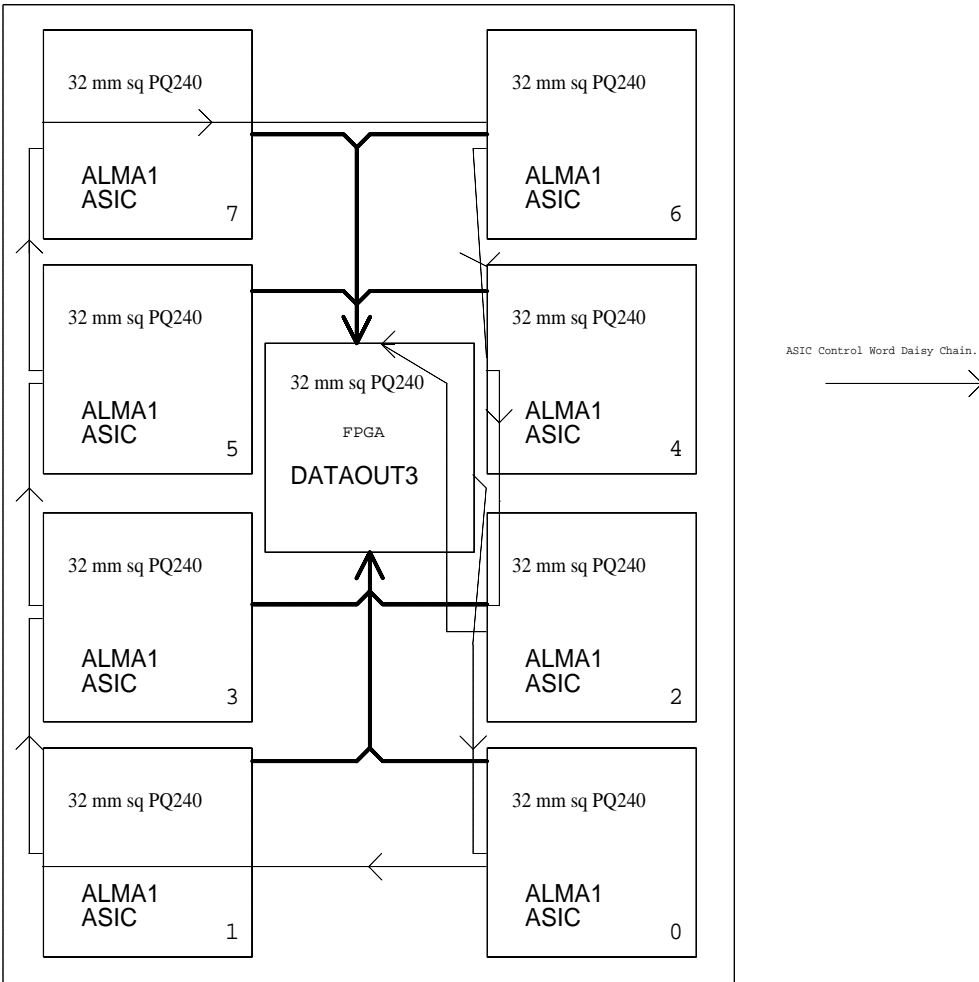
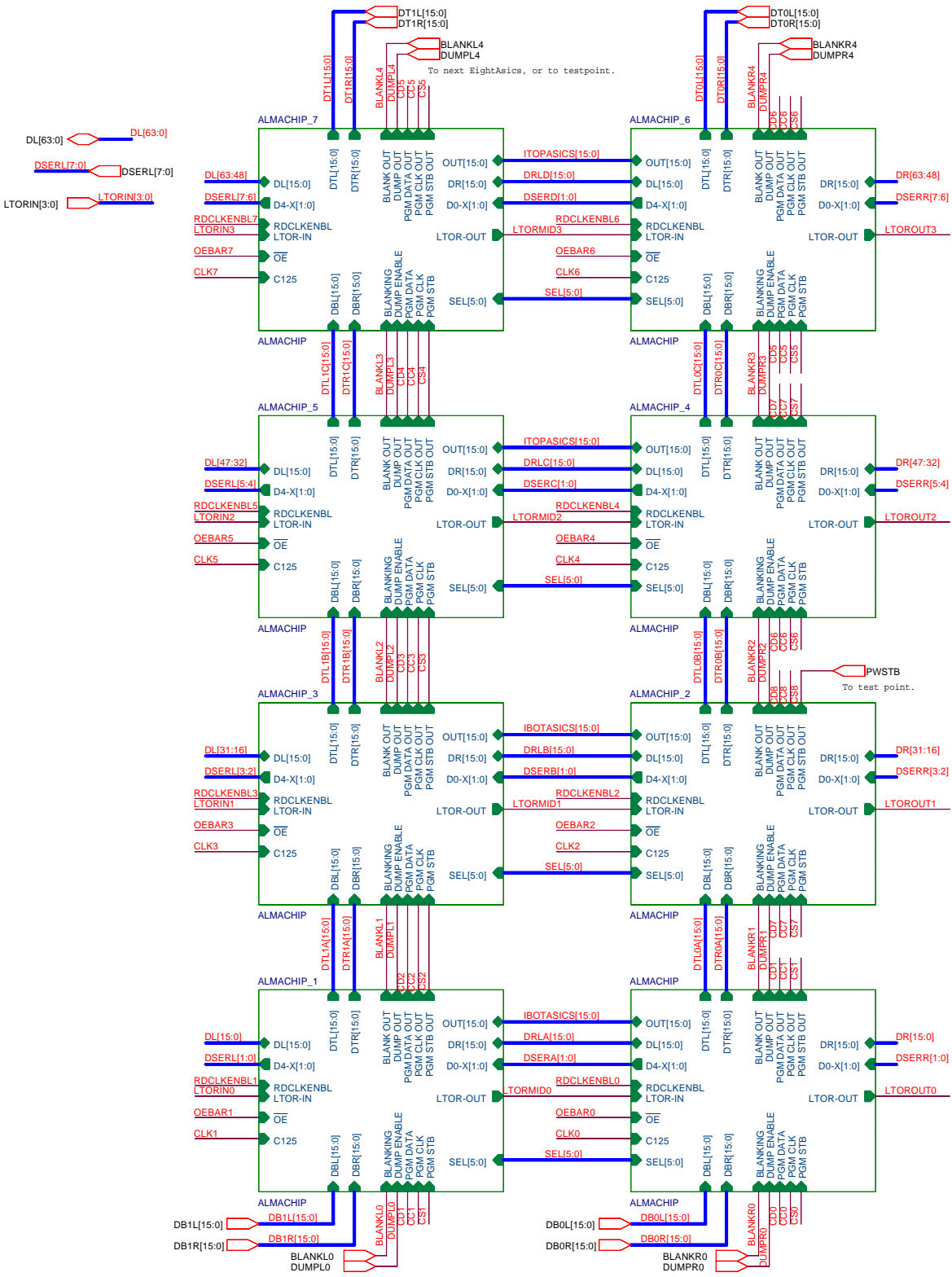
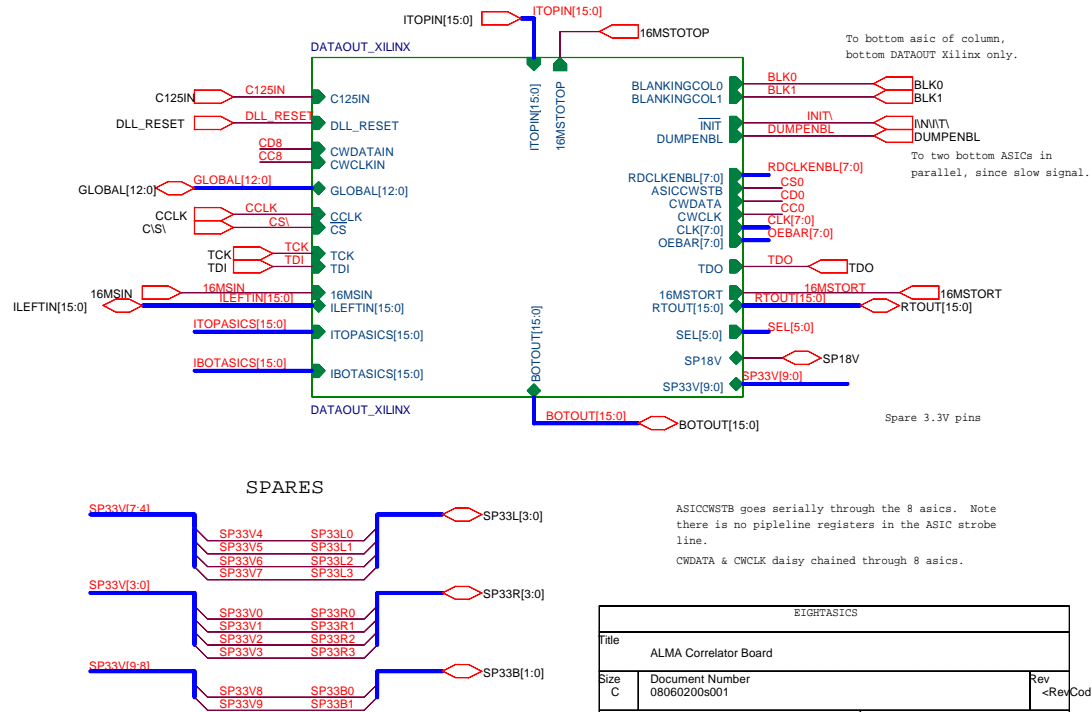


Each DATAOUT Xilinx is connected to eight ASICs, on the opposite side of the card, via two tri-state busses, as shown.



Control Words loaded in bottom ASICs first to allow for a partially populated card, with only the bottom row. Have vias positions such that a jumpers are possible from nets CD2 to CD8, and from CC2 to CC8.



EIGHTASICS	
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