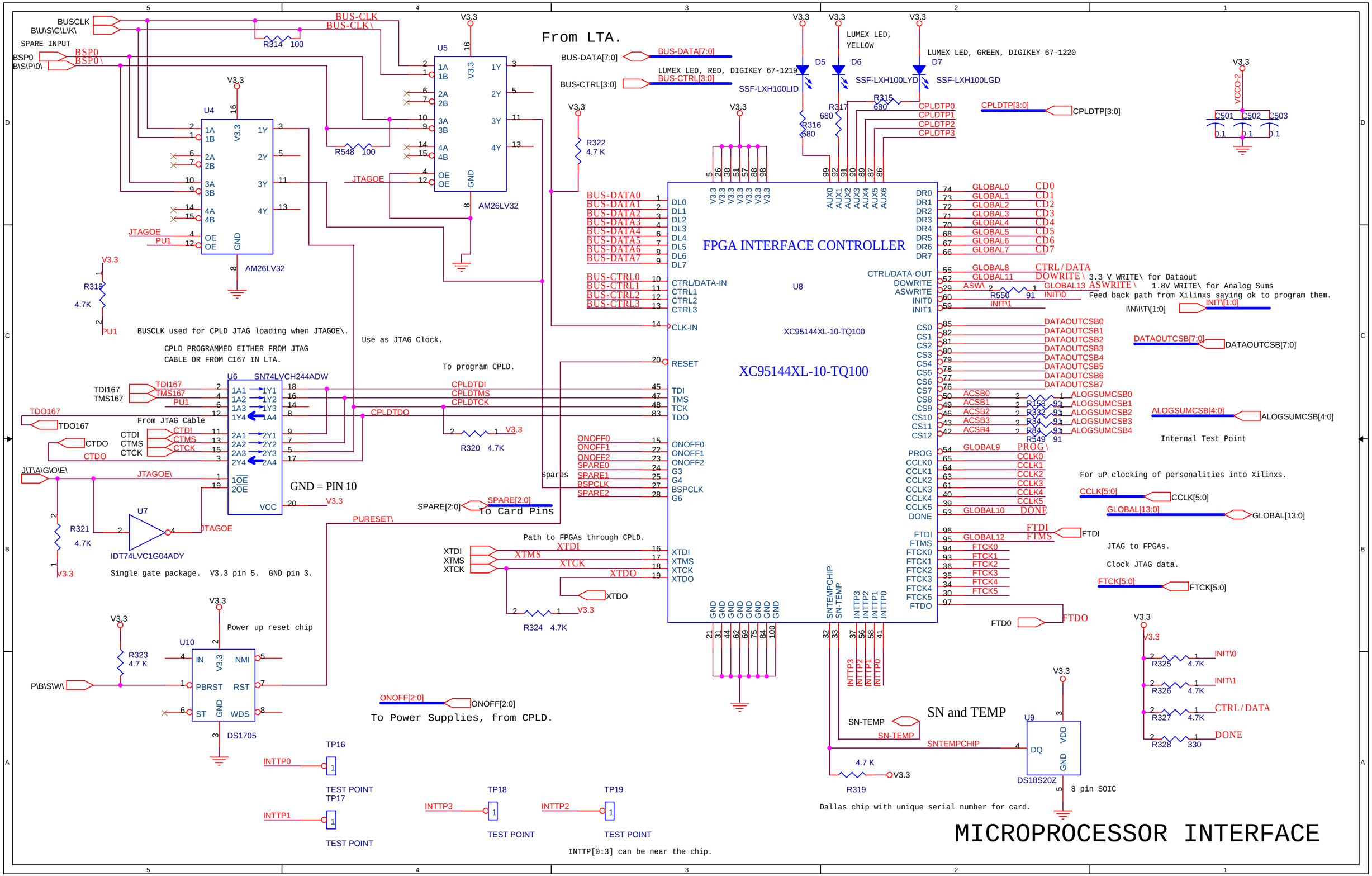
From LTA.
FPGA INTERFACE CONTROLLER
XC95144XL-10-TQ100
U8
U4
U5
AM26LV32
U6
SN74LVCH244ADW
GND = PIN 10
U7
IDT74LVC1G04ADY
Single gate package. V3.3 pin 5. GND pin 3.
U10
DS1705
Power up reset chip
U9
DS18S20Z
8 pin SOIC
SN and TEMP
Dallas chip with unique serial number for card.
BUSCLK used for CPLD JTAG loading when JTAGOE\.
CPLD PROGRAMMED EITHER FROM JTAG
CABLE OR FROM C167 IN LTA.
Use as JTAG Clock.
To program CPLD.
From JTAG Cable
To Card Pins
Path to FPGAs through CPLD.
To Power Supplies, from CPLD.
INTTP[0:3] can be near the chip.
Internal Test Point
For uP clocking of personalities into Xilinxs.
JTAG to FPGAs.
Clock JTAG data.
3.3 V WRITE\ for Dataout
1.8V WRITE\ for Analog Sums
Feed back path from Xilinxs saying ok to program them.
MICROPROCESSOR INTERFACE