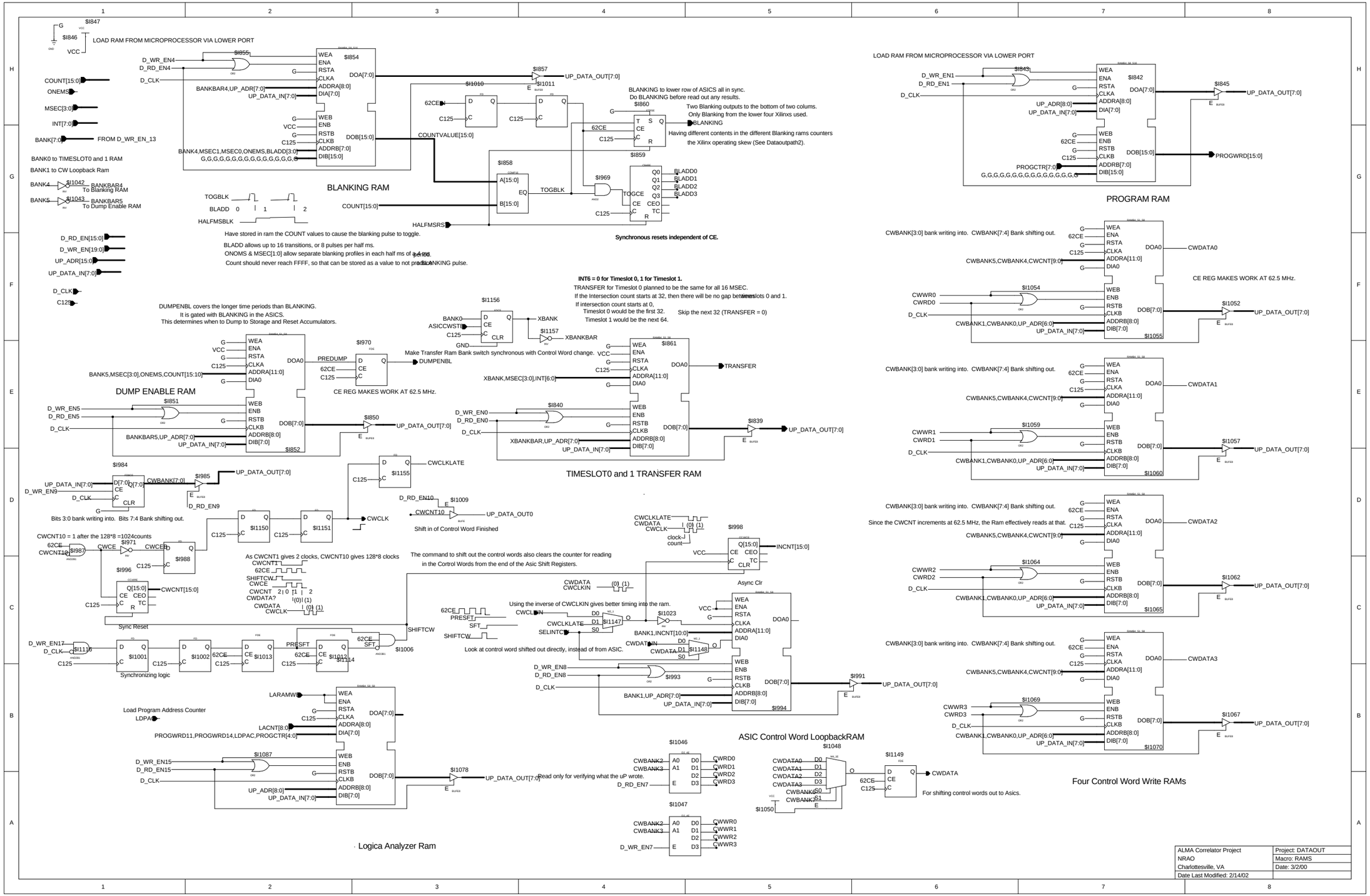
LOAD RAM FROM MICROPROCESSOR VIA LOWER PORT
BLANKING RAM
BANK0 to TIMESLOT0 and 1 RAM
BANK1 to CW Loopback Ram
To Blanking RAM
To Dump Enable RAM
FROM D_WR_EN_13
Have stored in ram the COUNT values to cause the blanking pulse to toggle.
BLADD allows up to 16 transitions, or 8 pulses per half ms.
ONOMS & MSEC[1:0] allow separate blanking profiles in each half ms of a period.
Count should never reach FFFF, so that can be stored as a value to not produce a BLANKING pulse.
BLANKING to lower row of ASICS all in sync.
Do BLANKING before read out any results.
Two Blanking outputs to the bottom of two colums.
Only Blanking from the lower four Xilinxs used.
Having different contents in the different Blanking rams counters
the Xilinx operating skew (See Dataoutpath2).
Synchronous resets independent of CE.
PROGRAM RAM
DUMPENBL covers the longer time periods than BLANKING.
It is gated with BLANKING in the ASICS.
This determines when to Dump to Storage and Reset Accumulators.
DUMP ENABLE RAM
CE REG MAKES WORK AT 62.5 MHz.
INT6 = 0 for Timeslot 0, 1 for Timeslot 1.
TRANSFER for Timeslot 0 planned to be the same for all 16 MSEC.
If the Intersection count starts at 32, then there will be no gap between timeslots 0 and 1.
If intersection count starts at 0,
Timeslot 0 would be the first 32.
Timeslot 1 would be the next 64.
Skip the next 32 (TRANSFER = 0)
Make Transfer Ram Bank switch synchronous with Control Word change.
TIMESLOT0 and 1 TRANSFER RAM
Bits 3:0 bank writing into. Bits 7:4 Bank shifting out.
Shift in of Control Word Finished
CWCNT10 = 1 after the 128*8 =1024counts
As CWCNT1 gives 2 clocks, CWCNT10 gives 128*8 clocks
The command to shift out the control words also clears the counter for reading
in the Cortrol Words from the end of the Asic Shift Registers.
Sync Reset
Synchronizing logic
Using the inverse of CWCLKIN gives better timing into the ram.
Look at control word shifted out directly, instead of from ASIC.
Load Program Address Counter
Read only for verifying what the uP wrote.
ASIC Control Word LoopbackRAM
Logica Analyzer Ram
CWBANK[3:0] bank writing into. CWBANK[7:4] Bank shifting out.
CE REG MAKES WORK AT 62.5 MHz.
Since the CWCNT increments at 62.5 MHz, the Ram effectively reads at that.
For shifting control words out to Asics.
Four Control Word Write RAMs
ALMA Correlator Project
NRAO
Charlottesville, VA
Date Last Modified: 2/14/02
Project: DATAOUT
Macro: RAMS
Date: 3/2/00