

IN EACH DATAOUT XILINX

In the Control data ram, an intersection is a 10 bit number, plus one control bit, telling if this Xilinx should actually dump data for this intersection, or just count.

All 8 Dataout Xilinx go through the same list simultaneously, each outputting only its intersections.

For Timeslot 0

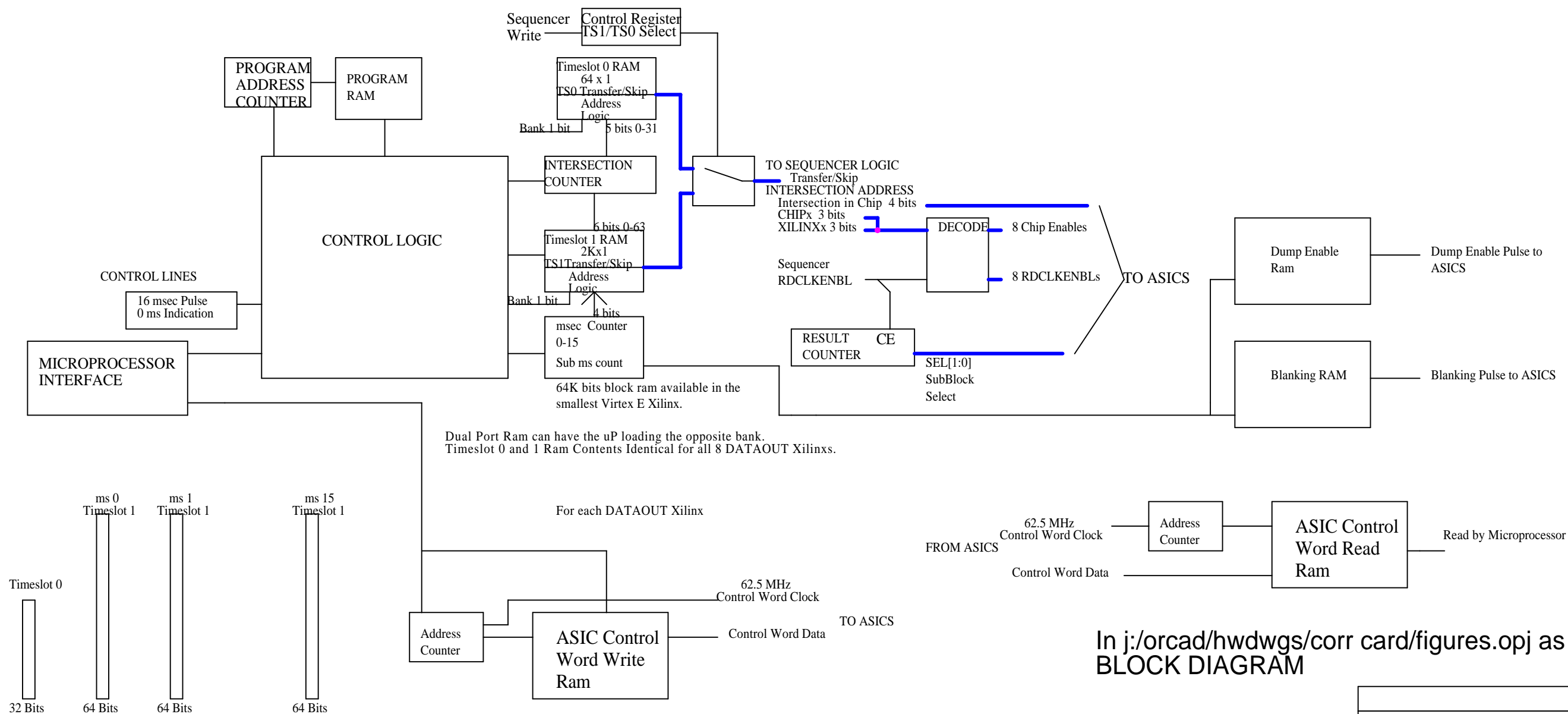
The 32 bits in the Timeslot 0 Memory represent the 32 possible diagonal intersections in the card. The subroutine will increment through the 32 bits. If Bit 0 says Skip, the routine will increment to the next bit. If Bit 0 says Transfer, and this bit is serviced by this Xilinx, the Xilinx will output the appropriate intersection. If Bit 0 says Transfer, and this bit is not serviced by this Xilinx, the Xilinx will pause to allow some other Xilinx to output an intersection.

For Timeslot 1

The 1024 intersections are divided into 16 sections of 64 intersections each. Each section represents the intersections serviced in a ms of the 16 ms cycle. Each ms represents the 64 intersections for 2 rows of antennas. The subroutine will increment through the 64 bits. If Bit 0 says Skip, the routine will increment to the next bit. If Bit 0 says Transfer, and this bit is serviced by this Xilinx, the Xilinx will output the appropriate intersection. If Bit 0 says Transfer, and this bit is not serviced by this Xilinx, the Xilinx will pause to allow some other Xilinx to output an intersection.

Each ms

Process Timeslot 0.
Process Timeslot 1 for the current ms.
Increment the ms counter.



In j:/orcad/hwdwgs/corr card/figures.opj as DATAOUT XILINX BLOCK DIAGRAM

Bit0-Transfer/Skip
Double buffer the above, to allow subarray switching.
Total storage = $(64 \times 16 + 32) \times 2 = 2112$ Bits

Note the same total system configuration is loaded in all 8 DATAOUT Xilinxs.

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ALMA Correlator Board		
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