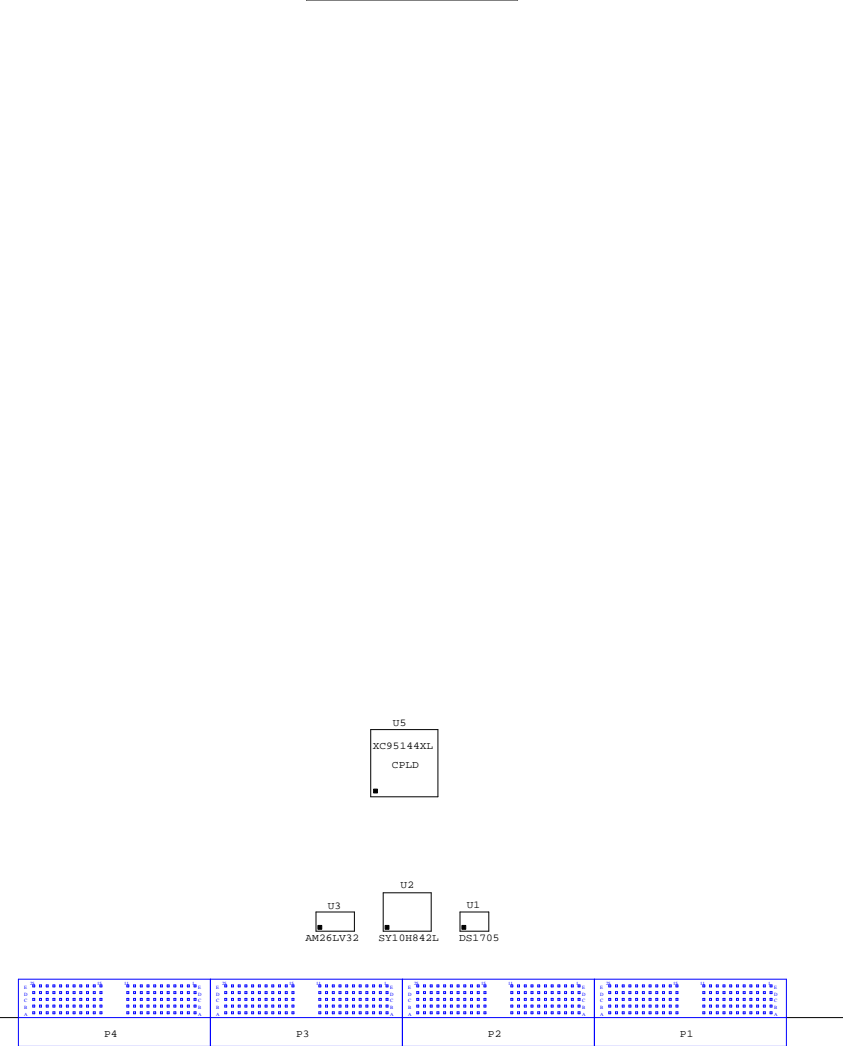
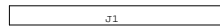


**TARGET CARD**

6U X 280 EURO-CARD  
 9.19" WIDE 11.02" HIGH



THE SIGNALS ABOVE ARE FTAG INPUTS THROUGH WHICH THE TARGET CARD'S FPGAs MAY BE LOADED WITH THEIR PERSONALITIES. THEY USE 3.3 VOLT LVCMOS LOGIC LEVELS THESE SIGNALS HAVE NO CONNECTION IN THE SYSTEM, THEY ARE TEST FIXTURE SIGNALS.

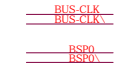
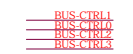
THE SIGNALS ABOVE ARE USED TO CONTROL THE FPGA INTERFACE CONTROLLER CELL OF THE TARGET CARD. THEY MAY BE USED TO LOAD THE CONTROLLER'S CPLD PERSONALITY VIA IT'S FTAG PORT. THE FTAG CLOCK, TCLK, IS DIFFERENTIAL AND THE RESET ARE SINGLE ENDED. ALL USE 3.3 VOLT LVCMOS LOGIC LEVELS.

THE PFSW SIGNAL IS A RESET INPUT FOR THE DALLAS SEMICONDUCTOR DS1705 MICRO MONITOR. IT CAN BE USED IF A RESET SIGNAL TO THE TARGET CARD IS NEEDED.



THE SIGNALS ABOVE ARE HIGH SPEED INTERFACE SIGNALS. SC125 IS THE SINK WAVE 125 MHz CLOCK AND STB IS THE 1 MSEC MEMORY CYCLE SYNCHRONIZATION SIGNAL. STB WILL BE A SHORT PULSE THAT WILL PROBABLY OCCUR EVERY 16 1.000 MSEC MEMORY CYCLES (THE EXACT DURATION AND REP-RATE WILL BE DECIDED LATER).

STB COMES FROM A XILINX FPGA OUTPUT ON THE CONTROL CARD WHICH HAS A 3.3 VOLT SUPPLY AND HAS A 110 OHM SERIES TERMINATION RESISTOR. A PARALLEL TERMINATION RESISTOR OF 91 OHMS ON THE TARGET CARD IS REQUIRED SO THE SIGNAL INPUT TO AN FPGA ON THE TARGET CARD CONFORMS TO 1.8 VOLT LVCMOS LOGIC LEVELS.



THE SIGNALS ABOVE PROVIDE A MICROPROCESSOR PORT TO THE TARGET CARD. THE BUS-DATA[7:0] SIGNALS ARE THE 8-BIT BI-DIRECTIONAL DATA BUS. THE BUS-CTRL[3:0] INPUTS ARE CONTROL SIGNALS. THE DIFFERENTIAL BUS-CLK SIGNAL IS THE PORT STROBE (RD + WR) SIGNAL. THE DIFFERENTIAL BSP0 IS A SPARE INPUT.

**CONTROL SIGNALS PROVIDED BY THE STATION CONTROL CARD TO A TARGET CARD.**

