

The ALMA Correlator

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ALMA Correlator Specifications

- 64 antennas
- 8 IF bands per antenna
- 4 Gsamples/sec per IF band, 2 bits/sample correlated
- 1024 lead + 1024 lag correlations per baseline
- 30 km maximum baseline delay range
- Full polarization capability plus autocorrelation
- Digital filter for bandwidths <2 GHz
- This requires 4,194,304 multiply-and-add correlators at 4 GHz rate
- Total computation rate is 1.7×10^{16} multiply-and-add operations/sec

ALMA Correlator

125 MHz Signal Interfaces

- Number of rack-to-rack signals over coax cables:
32,768
- Number of card-to-card signals over motherboards:
294,912

ALMA Correlator Outputs

- Accumulated auto- and cross-correlation sums
 - Summed from 32 cards processing 1/32 msec time slices
 - Accumulation times:
 - Auto: 1 msec to 8 msec, special mode
 - Cross + auto: 16 msec to 65 seconds
 - Output rates:
 - Up to 133 Mbyte/sec in each of 16 data streams
 - Maximum 2.1 Gbyte/sec (not supported by post-processing yet)
 - Initial support: perhaps 4 streams at up to 25 Mbyte/sec each
 - Sub-arrays: independent mode and accumulation time for each antenna; will not be the limiting factor for number of sub-arrays

ALMA Correlator Chip

- Chip specification complete
 - Fundamental cell: 64-lag correlator
 - Total of 4096 lags
 - Matrix arrangement for 2 X 2 inputs
 - Baseline design: 0.25 micron process @ 2.5 V
 - Expected power consumption <2 W
- Options
 - 0.18 micron process @ 1.3-1.8 V
 - 128-lag cell to give 8192 lags

ALMA Correlator Data Interfaces

- Use I/O pins of Xilinx Virtex-E FPGA chips
 - Specified to work at 300 MHz, will use at 125 MHz
 - 4-phase reclocking makes precise cable lengths irrelevant
 - Minimizes chip count and real estate (good)
 - Large, expensive chip connected to outside world (bad)
- Use Tensolite HM mass terminating coax
 - Factory pre-assembled ganged units
- Test assembly
 - Will verify configuration and performance margin
 - Final design of cards awaits tests

ALMA Correlator Status

- Station card: 90% of design done, waiting on I/O tests
- FIR filter: 90% of design done, waiting on I/O tests
- Correlator card: 20% of design done
- LTA: 40% of design done
- Control card: concept done, awaiting completion of requirements of other cards
- Test fixtures:
 - Station card/filter testing: 30% of design done
 - Correlator card testing: not started
 - Plan minimal card count complete correlator for debugging