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The ALMA Correlator Long Term Accumulator

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1 Introduction

This document describes the current functional specification of the Long Term Accumulator (LTA) being designed for the ALMA correlator. For purposes of this description, a 64-antenna ALMA system is assumed.

The input to the LTA is from short term integrations performed in the correlator chips. The short term integrator in the correlator chip can function in two fundamental modes:

21 Bit Integrator mode: 1.0 msec short term integrations in the correlator chip
25 Bit Integrator mode: 16.0 msec short term integrations in the correlator chip (see note below)

Three correlation modes are defined for sub-arrays in the correlator, using the two short term integration modes of the correlator chip:

Correlation Mode	Results Available	Short Term Integrations	Long Term Accumulation
Cross Correlation	Cross + Auto	25 bit, (16.0 msec)	Integer multiples of 16.0 msec
Auto Correlation	Auto	25 bit, (16.0 msec)	Integer multiples of 16.0 msec
Special Auto Correlation	Auto	21 bit, (1.0 msec)	None, sixteen 1.0 msec buffers

Note:

> There is some concern that the 16.0 msec basic interval for long term accumulations is not conveniently related to the 50.0 msec system cycle (the shortest common period is 400 msec). The short term integration interval is limited to a maximum of approximately 29 msec by the 25 bit integrator length. Thus a basic long term accumulation interval of up to 20 or 25 msec would be practical. Any smaller interval such as 10 msec would not be practical in the present design, where approximately 85% of the 16 msec is required for the LTA processing of correlator results. It should also be noted that the long term accumulation cycles must be integer multiples of the basic correlator 1.0 msec cycle (e.g. 12.5 msec would not be practical even if it provided enough time otherwise). The current consensus is that there is no need to change the 16.0 msec specification.

The accumulation section of the LTA is followed by an adder tree (described in Section 4). The outputs from the adder tree are considered to be the correlator output streams. These output streams drive a correlator to VME interface section in the VME rack. (The ALMA real time computer system is assumed here to consist of VME computers.)

2 LTA Specifications

The basic specifications of the LTA are:

- Sub-array support
    - Up to 16 independent sub-arrays
- Output binning support
    - for sub-arrays in Cross or Auto Correlation Mode (25 bit short term integration mode):

      1, 2 or 4 output bins, bin switching controlled on 16 msec boundaries
    - for sub-arrays in Special Auto Correlation Mode (21 bit short term integration mode):

      1 bin (no long term accumulation for 1.0 msec results)
- Accumulation times
    - for sub-arrays in Cross or Auto Correlation Mode (25 bit short term integration mode):

      Accumulation time can be specified in integer multiples of 16 msec:

      MINIMUM = 16 msec for 1 bin
32 msec for 2 bins
64 msec for 4 bins
(Minimum accumulation time is a function of the number of bins in use)

      MAXIMUM = approximately 65 seconds (maximum of 4096 accumulations of 16 msec results)
    - for sub-arrays in Special Auto Correlation Mode (21 bit short term integration mode):

      Accumulation time is fixed at 1 msec

      (16 buffers provided, so bank switch is every 16 msec, producing 16 consecutive sets of 1 msec auto products for each antenna in this mode)
- Data Format
    - LTA results are 32 bit unsigned integers.

- Correlator output streams
  - 16 streams total out of the full correlator system, into the output interface
  - 128 MByte/sec/stream capacity; (based on dumping 512 results from each of 1024 intersections of a 32 x 32 matrix in 16 msec)

- Output interface
  - Front Panel Data Port (FPDP) 32 bit parallel bus, 25 MHz clock (100 MByte/sec burst rate)
  - two FPDP for each correlator output stream (at 128 MByte/sec peak correlator stream output rate, the two FPDP streams then require operation at 64 MByte/sec peak)
  - 4 x 8 crossbar at each quadrant so results from any of the four output streams from one quadrant can be routed to any of eight VME FPDP input streams assigned to the quadrant, on a baseline basis, 32 VME input streams total
  - Transfer of correlator results over the interface sequenced automatically, as a function of sub-array mode parameters, each time a sub-array bank switch occurs.
  - Number of results transferred out of the correlator from each intersection is specified in multiples of 16 results per polarization data set (16 results minimum, 512 results maximum), on a sub-array basis;
(e.g. 16 results minimum per intersection in non-polarized mode; 32 minimum in dual polarization; 64 minimum in full polarization; 512 maximum in any mode)

- Timing
  - Independent control of data accumulation on 16 msec boundaries for each of the 16 sub-arrays

The 1 msec cycle is the fundamental blanking cycle in the correlator system. This blanking cycle is 125,000 system clock cycles (8 nsec per cycle), where correlation is blanked for some number of clock cycles out of every 125,000 clock cycles (blanked a minimum of 64, possibly as many as 512).

The proposed LTA design is based on a correlator chip that produces 8K lags (even though the actual chip may only produce 4K lags).

A single LTA (that handles all results from a single correlator card) will consist of one Field Programmable Gate Array (FPGA) and several Synchronous Dynamic Rams (SDRAM). The FPGA personality will be configurable for either 8K or 4K operation.

3 Correlator Cards, Planes and Arrays

In the discussion below, a correlator PLANE is defined as a 64-antenna times 64-antenna correlator matrix working at a clock rate of 125 MHz. A correlator plane processes 1/32 of the digitizer samples from a baseband pair (the two digitizers in a baseband pair each operate at a sample rate of 4 GS/SEC). A correlator plane consists of 4 printed circuit cards, where each correlator card implements a 32-antenna times 32-antenna correlator matrix.

Thirty-two correlator planes are required to process the full output of a baseband pair. A set of thirty-two planes is referred to as an ARRAY in the following text. The final correlator will contain four of these arrays, one of which is shown in Figure 1, ALMA Correlator Array.

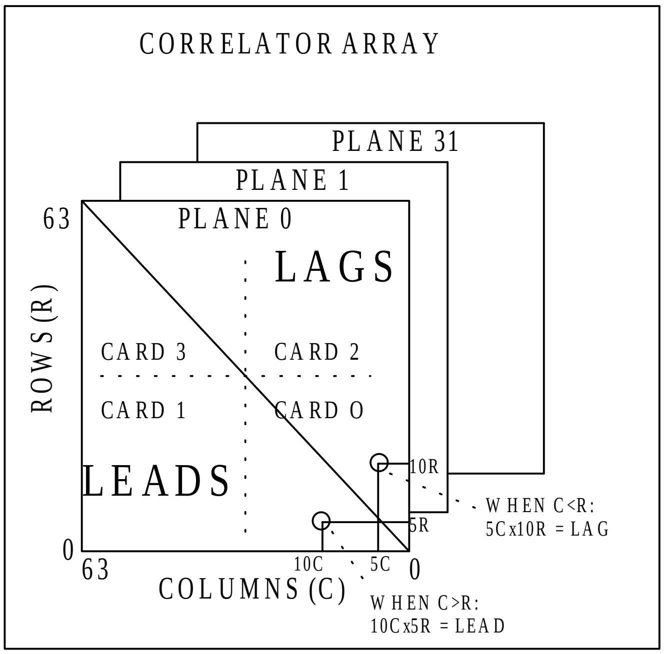

Figure 1, ALMA Correlator Array

Unsigned results (16 bits wide) from each correlator card are read out to a LTA over a single bus (one bus and LTA for each correlator card), at a burst rate of 16 nsec per result. The 16 bits are multiplexed over a physical 8 bit bus. Additionally, the correlator card will have a capability of high speed readout, with every result read out every 1 msec, over multiple buses, to multiple LTAs. In this case, the physical buses will be 16 bits wide, running at a burst rate of 8 nsec per result. This is an option for future expansion.

Cards 0 and 3 are referred to as SELF cards. Cards 1 and 2 are referred to as CROSS cards.

Each correlator card has 1,024 correlator blocks (32 x 32), and each block produces 512 sixteen bit wide results every integration period, for a total of 512K results per card. These correlator blocks are referred to as intersections. The total number of results in one card, one plane, one array and in the complete system of four arrays are:

PRODUCT	ONE NON-DIAG CARD	ONE DIAG CARD	ONE PLANE (2 diag + 2 non-diag cards)	ONE ARRAY (32 planes)	FOUR ARRAYS
AUTO	0	16,384	32,768	1,048,576	4,194,304
CROSS	524,288	507,904	2,064,384	66,060,288	264,241,152
TOTAL	524,288	524,288	2,097,152	67,108,864	**268,435,456**

(Total LTA ram storage for **268,435,456** results at 4 bytes per result = 1,073,741,824 bytes; when 4 bins and double buffering is provided, this produces a total of 8,589,934,592 bytes = 8 Gbyte total RAM memory distributed over 64 LTA cards in the entire system.)

3.1 Correlator Plane

Figure 2, One Correlator Plane , shows a set of four correlator cards, forming a single plane (1 of 32) of a correlator array, with the diagonal correlator chips highlighted. Each chip contains 16 intersections (an intersection produces 512 product results), and in each diagonal chip four of the intersections produce AUTO products (the intersections on the chip diagonal). All other intersections produce CROSS products. Each card contains 64 chips, labeled 0-63 in the figure.

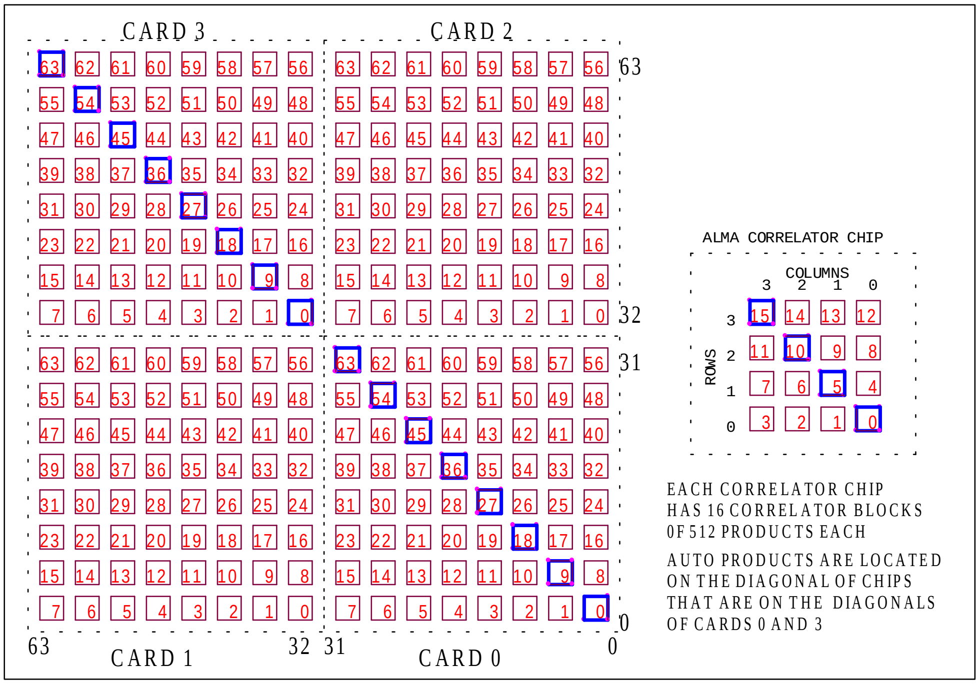

Figure 2, One Correlator Plane

4 LTA and Adder Tree

As shown in Figure 3 , LTA / ADDER TREE, each correlator card drives a LTA, and the output of each LTA goes to the first stage of an Adder Tree. A single Adder Tree is driven from the outputs of the 32 LTA that handle correlator card 0 in each of the 32 planes. The early stages of the adder tree are distributed over the four LTA cards, and the final stages are on a single Final Adder card. There are three other Adder Trees associated with the array, one each for card 1, card 2 and for card 3. Thus from one correlator array, there are four output streams, one from each of the four Adder Trees (only one shown in the figure). The adder tree inputs and outputs are 32 bit unsigned integers.

After every bank switch for a sub-array, results are available in the inactive LTA memory bank in each of the 32 planes in each of the four arrays, for transfer to the VME system. Depending on the baseband bandwidth, results from 2 or more planes may be added together in the adder tree, or results from all 32 planes may be transferred separately to the VME system, passing through the adder tree in a transparent manner.

At full bandwidth (2 GHz), all 32 planes must be summed together in order to produce 512 spectral channel results per intersection in each of the four arrays. At minimum bandwidth (62.5 MHz non-oversampled, 31.25 MHz oversampled), all 32 planes contain distinct lags, producing 16,384 spectral channel results per intersection in each of the four arrays. The spectral channels from each array could be for a single baseband, or split between the two basebands in a pair, or split into full polarization mode (RR, LR, RL, LL). The following table defines 6 adder tree modes as a function of baseband bandwidth and oversampling.

ADDER TREE MODE NUMBER	SPEC CHANS PRODUCED IN EACH ARRAY	BASEBAND BANDWIDTH NON-OVS	BASEBAND BANDWIDTH (OVERSAMPLED)
0	512	2 GHz	1 GHz
1	1024	1 GHz	500 MHz
2	2048	500 MHz	250 MHz
3	4096	250 MHz	125 MHz
4	8192	125 MHz	62.5 MHz
5	16384	62.5 MHz	31.25 MHz

Table 1, Adder Tree Modes

Each of the modes in the table above requires a different grouping of planes to be added together in the adder tree. Table 2, Groupings of Correlator Planes for each Adder Tree Mode, found at the end of this document, defines which planes must be added together to produce which spectral channels for each of the adder tree modes. The table includes a 32 bit mask for each entry. This mask specifies which planes will provide non-zero data into the adder tree, for a given transfer. For bits 0-31 in the mask, representing planes 0-31, a value of 1 in the mask bit indicates the data from the associated plane will be included in the sum. A value of 0 in the mask bit indicates the plane will not contribute to the sum.

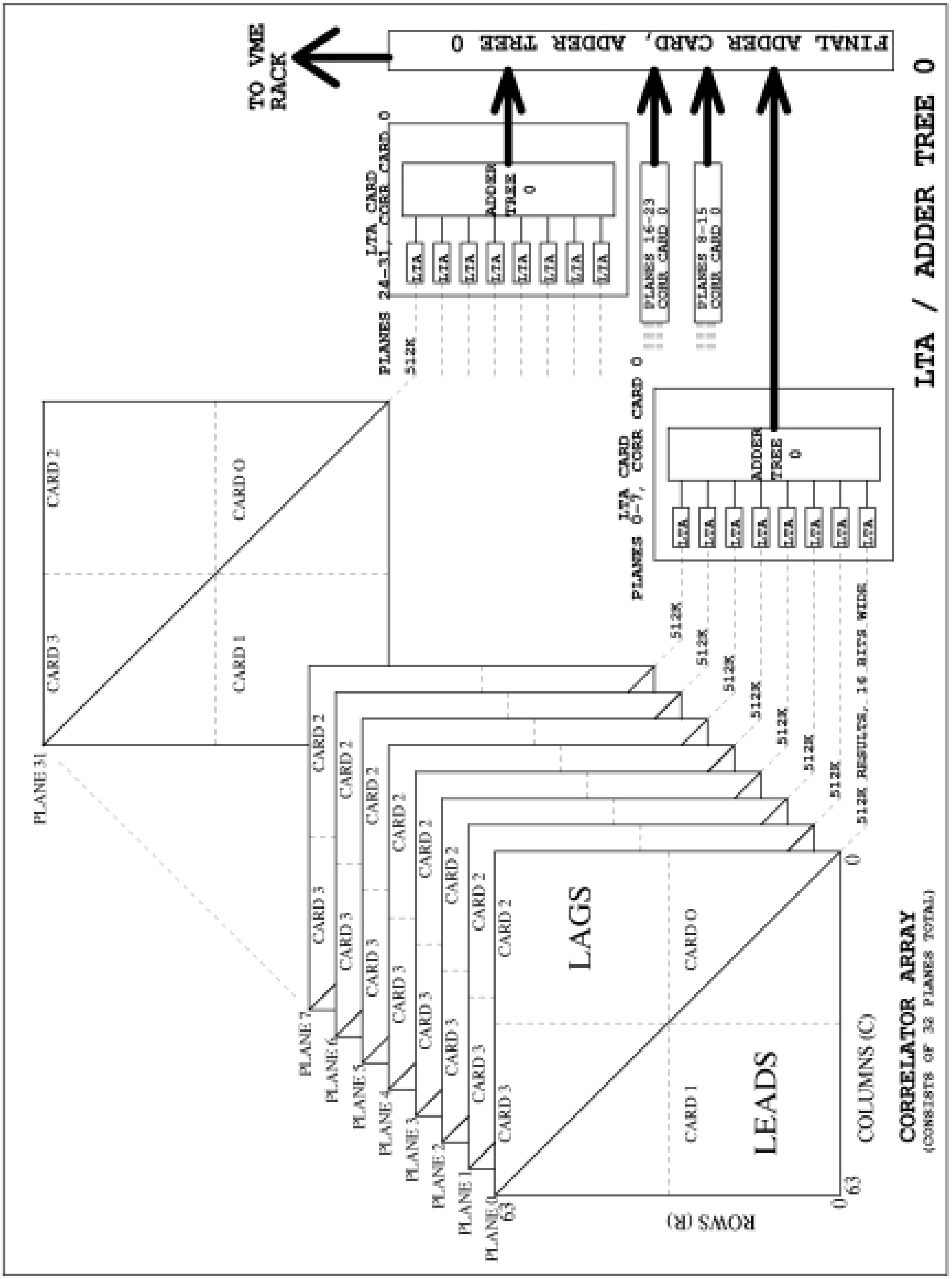

Figure 3 , LTA / ADDER TREE

5 Correlator Chip to LTA Data Transfers

Results are periodically dumped to secondary storage in the correlator chips, making the results available for possible transfer to the LTA.

Whether or not the results are actually transferred to the LTA, and how often, depends on the short term integration mode (25 or 21 bits) of the two antennas associated with an intersection and on whether the results are at a diagonal or non-diagonal intersection. (Note the term "diagonal" refers to the array diagonal, not to a correlator card diagonal. Thus diagonal intersections occur only on correlator cards 0 and 3, the SELF cards.)

5.1 Diagonal Intersections

For all diagonal intersections, dump to storage occurs every 16 msec if the associated antenna is in 25 bit short term integration mode, or every 1 msec if the antenna is in 21 bit mode.

- Results from diagonal intersections are always transferred to the LTA.

    a) Results from diagonal intersections in 25 bit mode are transferred every 16 msec.

    b) Results from diagonal intersections in 21 bit mode are transferred every 1 msec.

5.2 Non-Diagonal Intersections

For all non-diagonal intersections, dump to storage occurs every 16 msec.

- Results from non-diagonal intersections will transfer to the LTA only if the two antennas are both in 25 bit mode (either cross or auto correlation mode).

    a) These results are transferred every 16 msec.

    b) It is possible that the results might not be useful, in which case they will never be transferred out of the LTA, but results from all 25 bit x 25 bit non-diagonal intersections will always be transferred to the LTA.

    (The results will not be transferred out of the LTA if the antennas on the two axes are not in the same sub-array or if the antennas are in the same sub-array and the correlation mode is auto correlation mode.)

5.3 Transfer Timeslots

Each 1 msec interval will have two sub-intervals, referred to as timeslot 0 and timeslot 1. The 21 bit x 21 bit diagonal intersections will be transferred during timeslot 0, every 1 msec. The 25 bit x 25 bit intersections will be transferred during timeslot 1, distributed across a total of sixteen 1 msec intervals.

Figure 4, Sketch of 1 msec Blanking Cycle and Time Slots, shows the two timeslots. The time duration of the two timeslot intervals will vary as a function of the number of antennas in each of the two basic modes (21 and 25 bit).

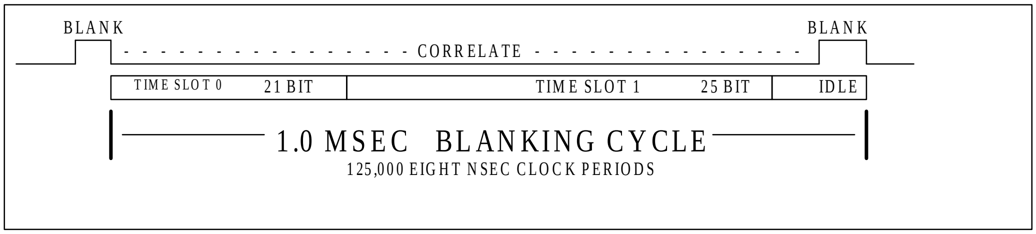

Figure 4, Sketch of 1 msec Blanking Cycle and Time Slots

The maximum number of results that must be transferred from either a SELF or CROSS card, in any 1 msec interval (including both timeslot 0 and timeslot 1), is 64 intersections of 512 results each for a total of 32,768 results. This is for the case where all 32 antennas on both axes of the correlator card are in 25 bit short term integration mode, in which case no results are transferred in timeslot 0, and timeslot 1 is fully subscribed every 1 msec (64 intersections transferred). With 64 intersections every 1 msec, a total of 1024 intersections are transferred in the full 16 msec interval (16 x 64 = 32 x 32 = 1024).

Diagonal intersections for antennas in 21 bit mode require 16 times the bandwidth of those in 25 bit mode. But this increase is more than compensated for by the fact that no results are transferred from non-diagonal intersections associated with an antenna in 21 bit mode.

Transfer of results from the correlator card is at a burst rate of 16 nsec per result. A basic interval of 48 system clock periods is used in the LTA to handle a set of 16 correlator results (an average of 24 nsec per result for each burst of 16 results). There is additional overhead required to provide refresh for the dynamic rams in the LTA. There are a minimum of 64 refreshes every 1 msec. Each refresh will be allocated 16 clock cycles.

5.4 Example Correlator to LTA Transfers

In the following examples, the diagonal intersections are evaluated for possible transfer of results during timeslot 0 of every 1 msec interval. Intersections in two pairs of columns are evaluated for possible transfer of results during each timeslot 1 of every 1 msec interval. Columns 0 and 1 are evaluated during timeslot 1 of 1 msec number 0, columns 2 and 3 during 1 msec number 1 etc. Over a full cycle of sixteen 1 msec intervals, all 32 columns on a correlator card are evaluated, two at a time.

5.4.1 SELF Card Transfers

For each antenna that is in 21 bit short term integration mode:

a) one intersection will be transferred during every timeslot 0

b) the number of intersections transferred during each timeslot 1will be reduced by more than the increase during timeslot 0

An example case can be seen in the figure below:

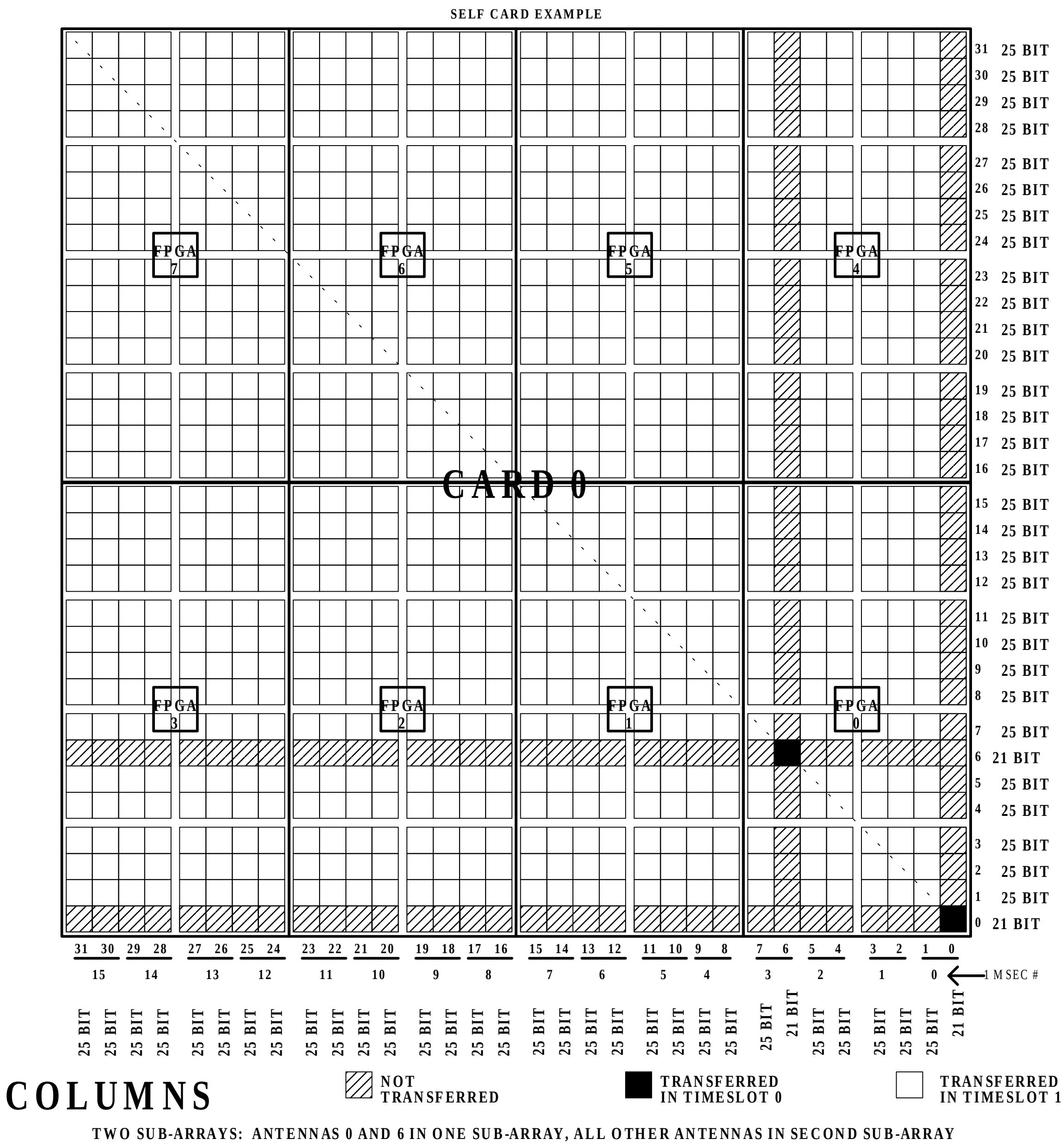

Figure 5 , Correlator to LTA Transfers, SELF Card Example

5.4.2 CROSS Card Transfers

For each antenna that is in 21 bit short term integration mode:

a) there are no timeslot 0 transfers (no diagonal intersections on cross cards)

b) the number of intersections transferred during each timeslot 1 will be reduced

An example case can be seen in the figure below:

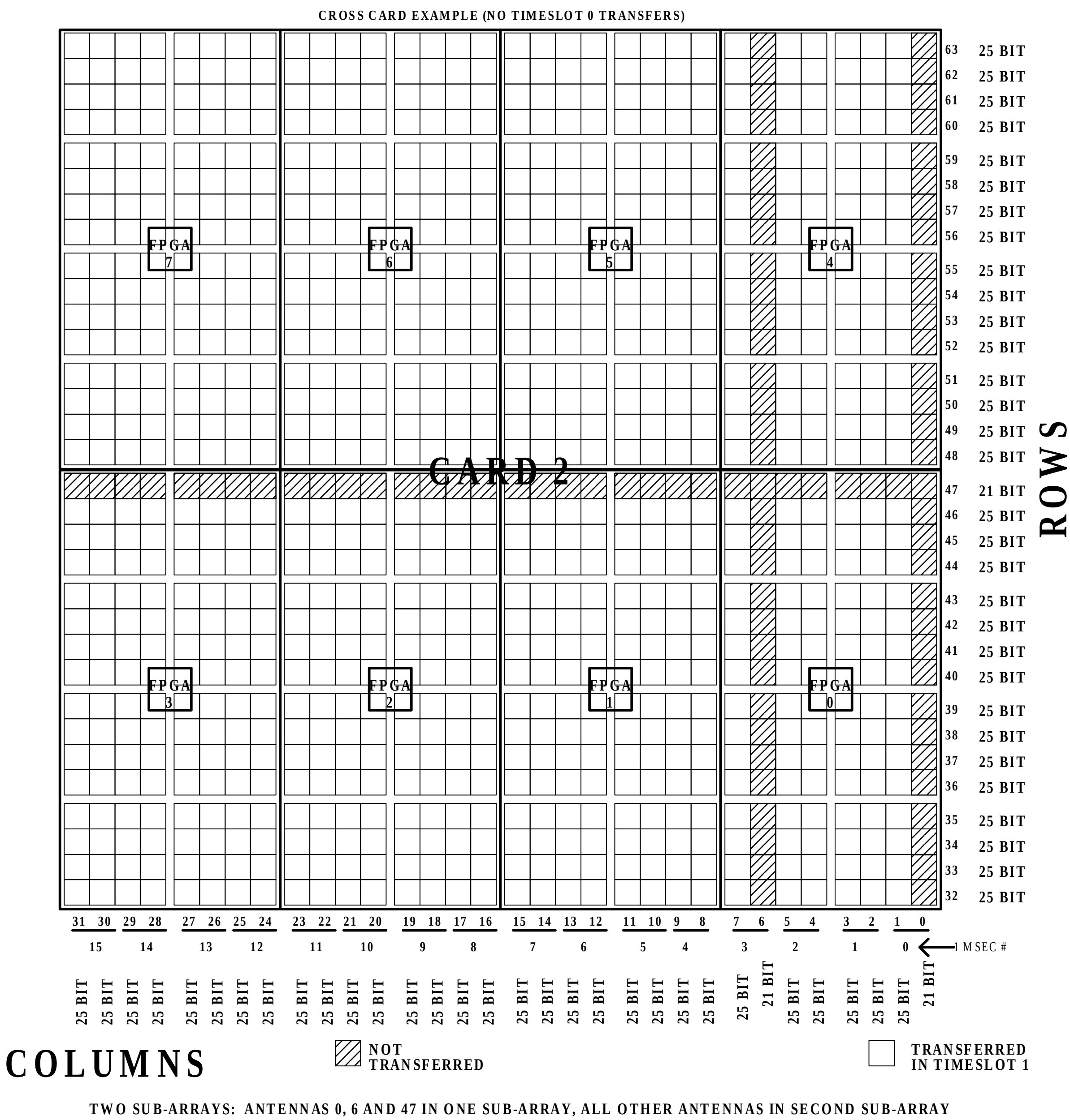

Figure 6, Correlator to LTA Transfers, CROSS Card Example

6 Correlation Modes and Correlator to VME Transfers

6.1 Cross Correlation Mode

For sub-arrays with antennas in this mode, useful results are produced at all sub-array intersections in the 64 x 64 correlator matrix. The correlator chips (both on and off the diagonal) use the 25 bit short term integrator option (16.0 msec short term integrations). Long term accumulation for all results is provided in the LTA, in multiples of 16 msec. All results (both diagonal and non-diagonal) are transferred out of the correlator system to the VME system.

6.2 Auto Correlation Mode

This mode is identical to cross correlation mode, except for the transfer of results out of the correlator system. Only the diagonal results are transferred out of the correlator system to the VME system.

6.3 Special Auto Correlation Mode

For sub-arrays with antennas in this mode, useful results are produced only on the diagonal of the 64 x 64 matrix. For all antennas in this mode, the correlator chips on the diagonal use the 21 bit short term integrator option (1.0 msec short term integrations). No long term accumulation is provided in the LTA. The LTA provides 16 buffers, so that sets of sixteen consecutive 1 msec results are stored and made available on 16 msec bank switch boundaries. Only these buffers of diagonal results are transferred out of the correlator system to the VME system.

7 Data Rates from the Correlator Cards and the LTA

7.1 LTA Input Data Rate In 25 Bit Short Term Integrator Mode

The maximum data rate from a single plane of correlator cards in one correlator array, when all antennas are in 25 bit short term integrator mode, is 2,097,152 results every 16 msec, or 128M results per second. At two bytes per result, this is 256 MByte/sec data rate from a single plane, 8 GByte /sec total from one array of 32 planes, and 32 GByte/sec total from all four arrays.

On a per card basis, there are 524,288 results per 16 msec. The data rate is thus 32M results per second, or 64 MByte/sec from each of four correlator cards in a plane (results are 16 bits wide).

7.2 LTA Input Data Rate In 21 Bit Short Term Integrator Mode

The maximum data rate from a single plane of correlator cards in one correlator array, when all antennas are in 21 bit short term integrator mode, is 32,768 results every 1 msec, or 32M results per second. At two bytes per result, this is 64 MByte/sec data rate from a single plane, 2 GByte/sec total from one array of 32 planes, and 8 GByte/sec total from all four arrays.

On a per card basis there are 16,384 results per 1 msec. The data rate is thus 16M results per second or 32 MByte/sec from the two SELF cards in a plane, and no data from the two CROSS cards.

7.3 LTA Output Data Rate and VME Interface

The LTA will be capable of an output transfer rate of 512 thirty-two bit results from a total of 1024 intersections every 16 msec, over each of 16 output streams from the full correlator. This is a transfer rate of 128 MByte/sec on a single output stream.

A standard 32 bit parallel interface, the Front Panel Data Port (FPDP) will be used to transfer data from the correlator to the VME system, eight FPDP per correlator quadrant (two per 32 x 32 matrix). Each FPDP will operate at a clock rate of 25 MHz, allowing a burst rate of 100 MByte/sec. A pair of FPDP interfaces is required for each of the 128 MByte/sec correlator output streams in order to support the maximum rate.

8 LTA and Adder Tree Internal Control

Each of the sub-arrays will have a correlation mode, accumulation time, and adder tree mode specified. As defined previously, supported accumulation times are integer multiples of 16 msec in cross and auto correlation mode, and a fixed accumulation time of 1 msec in special auto correlation mode. Accumulation for each sub-array will be capable of starting or stopping on 16 msec boundaries. Adder tree modes are those defined in Table 1 and in more detail in Table 2.

Each LTA card (handling results from 8 correlator cards) will maintain 16 bank switch counters, one per sub-array.

When a sub-array is in cross or auto correlation mode, the accumulation time N specifies the number of 16 msec intervals between bank switches (1, 2, 3 etc.). When the sub-array is in special auto correlation mode, the accumulation time is fixed at 1 msec, with 16 buffers provided, so the bank switch occurs every 16 msec, providing 16 buffers of 1 msec results.

A single micro controller will control the eight LTA on a single LTA/Adder Tree card. The micro controller will keep track of the parameters for each of 16 sub-arrays. Control of binning and bank switching will be implemented on a baseline basis (at each intersection), on 16 msec boundaries.

9 LTA Memory Space

Each LTA provides 4 bins of double buffered storage for every result on a correlator card. Correlator results are handled in pairs (e.g. lag 0 and lag 1 of an intersection are handled in parallel). There are 512 results for each of 1024 intersections on a correlator card. The pairs of results are stored in a 64 bit wide ram, 2 Meg deep (64 bits x 2 Meg = 128 Mbits = 512 results x 32 bits x 1024 intersections x 4 bins x 2 banks).

10 LTA and Adder Tree Cards

Figure 7, LTA and Adder Tree For One of Four Arrays, presents the planned implementation of the LTA and Adder Tree, for one quadrant, on a total of 20 cards. A single LTA function handles one Correlator Card. The sixteen LTA/ADDER TREE cards shown in the figure each contain 8 LTA providing a total of 128 LTA functions plus the initial stages of the adder tree. Four additional cards contain the final adder stages for each 32 x 32 matrix and connect to a card containing the output FIFOs, 4 x 8 crossbar, and FPDP interfaces to the VME system.

11 VME Control of LTA

Each LTA requires the sub-array assignment (0-15) for the 32 antennas on the ROW axis and the 32 antennas on the COLUMN axis of the 32 x 32 matrix handled by the LTA, along with sub-array parameters (e.g. correlation mode and accumulation time). The output stream assignment (1 of 8) for each intersection is also required at the output crossbar. It is presently expected that the CAN bus will be used for transfer of this control data.

Additional commands to be passed over the CAN bus, from the VME system to the LTA cards, are the start and stop accumulation commands. Upon receipt of the start accumulation command for a sub-array, any new parameters (e.g. correlation mode and accumulation time) will be made effective at the next 16 msec boundary. Upon receipt of the stop accumulation command, a final bank switch will be executed at the next 16 msec boundary and further bank switches will be inhibited.

12 Maximum Accumulation Time and Overflow

Correlator results are unsigned, 16 bits wide (0 – 65,535) and are accumulated into a 32 bit unsigned format in the LTA. The adder tree inputs and outputs retain this 32 bit unsigned format.

If we look at a worst case where 16 bits of all one's are accumulated every 16 msec, for a total of 65.536 seconds (4096 accumulations), the 32 bit LTA result field does not overflow. But if this occurs in 32 planes that must be added together, the adder tree 32 bit field does overflow by a factor of 2. Thus the specification of 65 seconds does not safely include this worst case. In such a case, multiple bins could be used to prevent overflow from occurring.

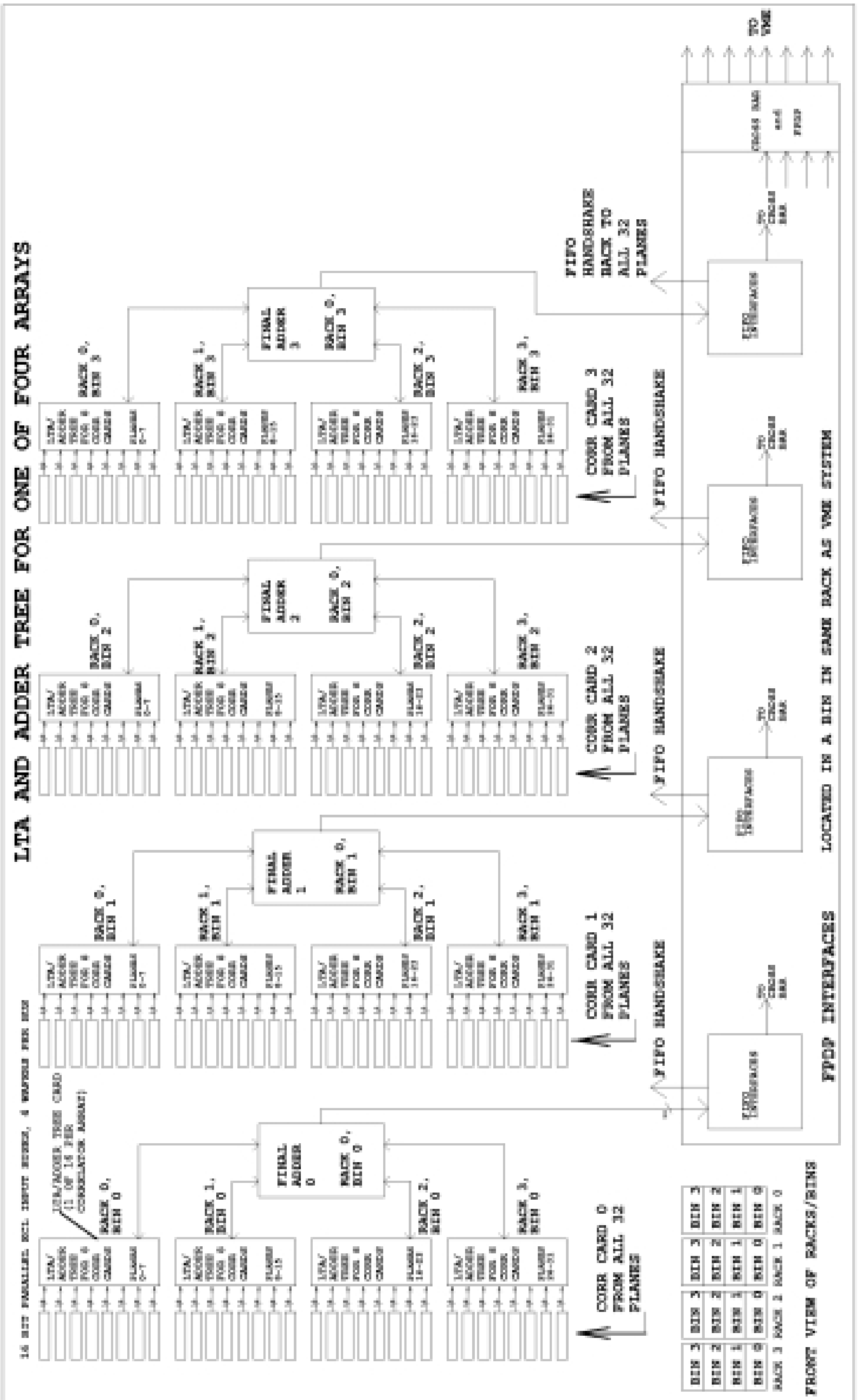

Figure 7, LTA and Adder Tree For One of Four Arrays

13 FPDP Data Transfers LTA to VME

At every bank switch boundary for each active sub-array, results from the sub-array will be transferred to the VME system. The transfers will be automatic and controlled by parameters associated with each sub-array. The available bandwidth over the FPDP interface will be shared among the sub-arrays every 16 msec. One control parameter will specify the number of intersections per sub-array to be transferred every 16 msec, following a bank switch, (as long as there are results remaining to be transferred).

We define the total number of intersection transfers based on how many times a single intersection must be considered for transfer from a set of 32 planes. For example, in adder tree mode 0, we add together the results from the intersections in all 32 planes, while in adder tree mode 5, we must transfer 32 distinct sets of results, one set per plane, for an intersection. If more than one bin is being used, then this also increases the number of individual transfers for an intersection.

For a given sub-array, the total number of intersection transfers out of an Adder Tree is calculated as a function of the number of antennas on the ROW and/or COLUMN axes that are assigned to the sub-array, the adder tree mode and the number of bins as follows:

(the 2 ^ ADDER_TREE_MODE term in the equations below evaluates to a value of 1, 2, 4, 8, 16 or 32 where the ADDER_TREE_MODE value is defined to be one of 0, 1, 2, 3, 4 or 5 as seen in Table 2, Groupings of Correlator Planes for each Adder Tree Mode)

SELF CARD ADDER TREE OUTPUTS:

CROSS Correlation Mode sub-arrays

Total # intersection transfers = (#COLs ^ 2) x (2 ^ ADDER_TREE_MODE) x (#BINS)
(all diagonal and non-diagonal intersections transferred, for every pairing of antennas in the sub-array)

AUTO Correlation Mode sub-arrays

Total # intersection transfers = (#COLs) x (2 ^ ADDER_TREE_MODE) x (#BINS)
(only the diagonal intersections transferred, for each antenna in the sub-array)

Special AUTO Correlation Mode sub-arrays

Total # intersection transfers = (#COLs x 16) x (2 ^ ADDER_TREE_MODE)
(16 buffers of 1 msec diagonal intersections transferred for each antenna in the sub-array)

CROSS CARD ADDER TREE OUTPUTS:

CROSS Correlation Mode sub-arrays

Total # intersection transfers = (#ROWs x #COLs) x (2 ^ ADDER_TREE_MODE) x (#BINS)
(all intersections transferred, for every pairing of antennas in the sub-array)

AUTO Correlation Mode sub-arrays

No results to transfer

Special AUTO Correlation Mode sub-arrays

No results to transfer

The number of intersection transfers per 16 msec tic for each sub-array is calculated as follows:

#PER_TIC >= ceil (TOTAL_NR_INTERSECTIONS / NR_16msec_TICS)

where the ceil(x) function is a C function that returns the smallest integral value not less than x, and the NR_16msec_TICS is the accumulation time for the sub-array (in terms of the number of 16 msec tics).

Also associated with each sub-array will be the number of results per intersection per polarization set. This will be a minimum of 16 results from each polarization set.

The maximum number of intersection transfers in 16 msec, for the sum of all sub-arrays, is 1024. This corresponds to the maximum number of transfers from a correlator card to the LTA from a single plane. At present, we do not know of any modes where more than 1024 intersection transfers from LTA to VME would be required in 16 msec.

FIFO buffering will be provided in each output stream. At the start of every 1 msec interval, the FIFO status will be checked to determine if there is room for a full 1msec of results (64 intersections x 512 results = 32K). If this is not the case, then transfers will be skipped for that 1 msec interval. A check will be made each time there is a bank switch in the LTA to determine if the results from the previous bank switch were all transferred.

The 4 x 8 crossbar at each quadrant, providing 8 FPDP interfaces into one or more VME systems, provides the capability of handling the full LTA output capacity of 128 MByte/sec on each of four streams by distributing the data over eight streams, each running at 64 MByte/sec (FPDP clock at 25 MHz, for 100 MByte/sec burst rate).

Each intersection will be assigned to one of the eight correlator to VME output streams in a quadrant. Each set of results from an intersection will be tagged with a header to identify the block of data. This tag may be useful in de-bugging. The header should not be necessary in normal operation, since the sequence of results every 16 msec should be entirely predictable.

Each sub-array will be specified as either non-polarized (one set of data), dual polarization (two sets of data), or full polarization (four sets of data).

14 Combining LTA and Correlator Control Card

As described previously, there will be a total of 16 LTA cards in one correlator array (a set of four racks, four bins per rack, one LTA per bin). The LTA card will also include the control functions for the correlator cards located in the same bin as the LTA. Thus each LTA/CCC (Correlator Control Card) will require certain parameters for all 64 antennas. Each of the 16 LTA/CCC requires the exact same set of parameters, so a broadcast mechanism on the control interface is perhaps appropriate.

Table 2, Groupings of Correlator Planes for each Adder Tree Mode

MODE 0 (2 GHz)	SPEC CHANS	MASK	MASK NR
0+1+2+3+4+5+………….+25+26+27+28+29+30+31	0-511	0xFFFFFFFF	0

MODE 1 (1 GHz)	SPEC CHANS	MASK	MASK NR
0+2+4+6+8+10+12+14+16+18+20+22+24+26+28+30	0-511	0x55555555	1
1+3+5+7+9+11+13+15+17+19+21+23+25+27+29+31	512-1023	0xAAAAAAAA	2

MODE 2 (500 MHz)	SPEC CHANS	MASK	MASK NR
0+4+ 8+12+16+20+24+28	0- 511	0x11111111	3
1+5+ 9+13+17+21+25+29	512-1023	0x22222222	4
2+6+10+14+18+22+26+30	1024-1535	0x44444444	5
3+7+11+15+19+23+27+31	1536-2047	0x88888888	6

MODE 3 (250 MHz)	SPEC CHANS	MASK	MASK NR
0 + 8 + 16 + 24	0- 511	0x01010101	7
1 + 9 + 17 + 25	512-1023	0x02020202	8
2 + 10 + 18 + 26	1024-1535	0x04040404	9
3 + 11 + 19 + 27	1536-2047	0x08080808	10
4 + 12 + 20 + 28	2048-2559	0x10101010	11
5 + 13 + 21 + 29	2560-3071	0x20202020	12
6 + 14 + 22 + 30	3072-3583	0x40404040	13
7 + 15 + 23 + 31	3584-4095	0x80808080	14

MODE 4 (125 MHz)	SPEC CHANS	MASK	MASK NR
0 + 16	0- 511	0x00010001	15
1 + 17	512-1023	0x00020002	16
2 + 18	1024-1535	0x00040004	17
3 + 19	1536-2047	0x00080008	18
4 + 20	2048-2559	0x00100010	19
5 + 21	2560-3071	0x00200020	20
6 + 22	3072-3583	0x00400040	21
7 + 23	3584-4095	0x00800080	22
8 + 24	4096-4607	0x01000100	23
9 + 25	4608-5119	0x02000200	24
10 + 26	5120-5631	0x04000400	25
11 + 27	5632-6143	0x08000800	26
12 + 28	6144-6655	0x10001000	27
13 + 29	6656-7167	0x20002000	28
14 + 30	7168-7679	0x40004000	29
15 + 31	7680-8191	0x80008000	30

MODE 5 (62.5 MHz)	SPEC CHANS	MASK	MASK NR
0	0- 511	0x00000001	31
1	512-1023	0x00000002	32
2	1024-1535	0x00000004	33
3	1536-2047	0x00000008	34
4	2048-2559	0x00000010	35
5	2560-3071	0x00000020	36
6	3072-3583	0x00000040	37
7	3584-4095	0x00000080	38
8	4096-4607	0x00000100	39
9	4608-5119	0x00000200	40
10	5120-5631	0x00000400	41
11	5632-6143	0x00000800	42
12	6144-6655	0x00001000	43
13	6656-7167	0x00002000	44
14	7168-7679	0x00004000	45
15	7680-8191	0x00008000	46
16	8192-8703	0x00010000	47
17	8704-9215	0x00020000	48
18	9216-9727	0x00040000	49
19	9728-10239	0x00080000	50
20	10240-10751	0x00100000	51
21	10752-11263	0x00200000	52
22	11264-11775	0x00400000	53
23	11776-12287	0x00800000	54
24	12288-12799	0x01000000	55
25	12800-13311	0x02000000	56
26	13312-13823	0x04000000	57
27	13824-14335	0x08000000	58
28	14336-14847	0x10000000	59
29	14848-15359	0x20000000	60
30	15360-15871	0x40000000	61
31	15872-16383	0x80000000	62