ALMA Memo 337

Development of Frequency Multiplier Technology for ALMA

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This ALMA memo, also published as a dissertation at the University of Virginia in January 2003 (UVA Science Engineering Library call number Diss. Engr. 2003.S24), presents a novel GaAs on Quartz based approach toward larger band-width Schottky diode frequency multipliers and reports the first fully integrable frequency multiplier based on this composite substrate is reported. This technology was developed as a low cost solution for meeting the ALMA frequency multiplier requirement up to about 400 GHz.

This technology has since then been commercially applied to design and build frequency triplers for the first local oscillator chains for ALMA bands 6 and 7.

The memo also describes other contemporary state-of-the-art frequency multiplier technologies and provides a comprehensive up to date survey of existing frequency multiplier designs together with their measured performances from published literature.

Abstract

A key requirement for the operation of a super-heterodyne millimeter- and submillimeter- wave receiver is the availability of a local oscillator (LO) signal used to pump a non-linear component such as a low noise superconductor-insulator-superconductor (SIS) junction, a Schottky-diode, or a Hot Electron Bolometer (HEB) device that down-converts the received Radio Frequency (RF) signal. Frequency multipliers have been used for many years to produce the required LO power. Traditionally, these frequency multipliers have been "hybrid" circuits, designed around planar discrete diode array packages fabricated on tiny pieces of semiconductor (GaAs, InP) material. The diode packages are attached to embedding circuitry usually fabricated on a low dielectric material like quartz. This approach, while highly successful up to about 100 GHz, has inherent drawbacks (of process, parasitic and performance variabilities, as well as being labor intensive) that limits its applicability for higher frequencies.

This dissertation describes the design, fabrication and evaluation of three frequency multipliers: The 55/110 GHz and the 110/220 GHz frequency doublers and the 80/240 GHz frequency tripler. The frequency doublers were designed based on the hybrid-circuit approach and illustrate the limitations of extending this approach to design frequency multipliers for frequencies

above 100 GHz. The 80/240 GHz frequency tripler was designed to be fully integrable and used diode chips that were fabricated on a composite substrate comprising of GaAs-membrane-on-quartz, suitable for the fabrication of linear embedding circuitry alongside the diodes on the same chip. This is the first reported frequency multiplier to 1) use the UVA GaAs-membrane-on-quartz process to implement balanced diode configuration with an integrated and optimized idler loop, 2) innovatively use an air-gap in the microstrip transmission line to synthesize a high-quality series negative reactance tuning element, and 3) use 1 mil thick fused-quartz substrate for linear embedding circuitry. This approach circumvents the "dielectric loading" problems of GaAs-based MMIC multipliers as well as the fragile nature of the rather large thinned-substrate or membrane type MMICs that are more suited to applications beyond 300 GHz.

The first experimental study of planar capacitor and spiral inductors, to gauge their applicability for high frequency multiplier MMIC work, was also a part of this research. The final part of the research focused on analytical and simulation based study to characterize the sideband noise transmission characteristics of diode based frequency multipliers. These noise characteristics are important, particularly in cases where the un-filtered output of a frequency multiplier is used to pump a frequency converter having a large IF bandwidth (often the case in millimeter- and submillimeter- wave receivers).

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A	Contact area of a diode junction.
C_{fp}	Finger − to − pad parasitic capacitance in a planar diode geometry.
C_{j0}	Zero bias junction capacitance of a diode, equivalent to $\mathrm{C_j(V_j = 0)}$.
$C_j(V_j)$	Capacitance of a diode junction. (Function of the potential difference across the junction.)
C_{pp}	Pad − to − pad parasitic capacitance in a planar diode geometry.
E	Electric field. (Exception : In Chapter − 5, due to a lack of better notation, this symbol has been used to represent time dependant amplitude of a noisy input pump signal to a frequency multiplier.)
$I(t)$	Electric current. (Function of time.)
I_0	Reverse saturation current of a Schottky junction or diode.
$I_L(t)$	Current in the "load" termination. (Function of time.)
I_{max}	Velocity saturation limited drift current.
$I_n(t)$	Electric current. (Function of time.)

$K_{\pm n,\pm 1}(f)$	Transmission coefficients relating the sidebands of the Fourier spectrum of the output voltage waveform of a frequency multiplier to the sidebands of the Fourier spectrum of the input voltage waveform. (Function of frequency.)
L_f	Inductance of the bridge or finger metalization in a planar diode geometry.
N_{buffer}	Doping concentration of the buffer layer in a diode.
N_d	Doping concentration of the epitaxial layer in a diode.
P	Power.
P_{in}	Available input pump power to a frequency multiplier.
P_{out}	Available output power of a frequency multiplier.
$Q(V)$	Charge stored in a Schottky junction. (Function of electric potential difference across the junction.)
R_{buffer}	Resistance of the buffer layer.
R_{epi}	Resistance of the undepleted epitaxial layer.
R_j	Parasitic (leakage) resistance of a diode junction.
R_{ohmic}	Resistance of the ohmic contact between the buffer layer and the contact metalization for the terminal.
R_{spread}	Spreading resistance to account for the ohmic losses arising in the buffer layer as the vertical column of current spreads out into the bulk of the buffer region.
R_s	Total parasitic series resistance of a diode.
$\mathbf{S_e}(\mathbf{f})$	The noise power spectrum matrix of the input pump signal to a frequency multiplier.

$S_e^{aa}(f)$ Element of the input power spectrum matrix, represents the amplitude noise spectrum of the signal.

$S_e^{a\phi}(f)$ Element of the input power spectrum matrix, represents the cross − correlation between the amplitude noise spectrum and the phase noise spectrum of the signal.

$S_e^{\phi a}(f)$ Element of the input power spectrum matrix, represents the cross − correlation between the phase noise spectrum and the amplitude noise spectrum of the signal.

$S_e^{\phi\phi}(f)$ Element of the input power spectrum matrix, represents the phase noise spectrum of the signal.

S_{ij} Component of the S − parameter matrix of a network representing a measure of the outgoing voltage wave amplitude at port − i due to an incident voltage wave at port − j.

$\mathbf{S_v(f)}$ The noise power spectrum matrix of the output signal from a frequency multiplier.

$S_v^{aa}(f)$ Element of the output power spectrum matrix, represents the amplitude noise spectrum of the signal.

$S_v^{a\phi}(f)$ Element of the output power spectrum matrix, represents the cross − correlation between the amplitude noise spectrum and the phase noise spectrum of the signal.

$S_v^{\phi a}(f)$ Element of the output power spectrum matrix, represents the cross − correlation between the phase noise spectrum and the amplitude noise spectrum of the signal.

$S_v^{\phi\phi}(f)$ Element of the output power spectrum matrix, represents the phase noise spectrum of the signal.

$\mathbf{T(f)}$	The noise transmission matrix of a frequency multiplier. (Function of frequency.)
T_{aa}	Element of the noise transmission matrix relating the output amplitude noise with the input amplitude noise.
$T_{a\phi}(f)$	Element of the noise transmission matrix relating the output amplitude noise with the input phase noise. (Function of frequency.)
$T_{\phi a}$	Element of the noise transmission matrix relating the output phase noise with the input amplitude noise.
$T_{\phi\phi}(f)$	Element of the noise transmission matrix relating the output phase noise with the input phase noise. (Function of frequency.)
V	Electric potential or voltage. Also used to represent the amplitude of a voltage waveform.
V_{bi}	Built in potential of a diode junction.
V_{br}	Reverse breakdown voltage of a diode.
V_d	Potential or voltage difference across the diode terminals.
V_j	Potential or voltage difference across a diode junction.
V_s	emf of a voltage source.
Z	Impedance.
Z_L	Load impedance.
Z_{SHORT}	Actual impedance of a practical short circuit.
$Z_{emb}(f)$	Embedding impedance. (Function of frequency.)
Z_g	Internal impedance of a voltage generator, used to drive a frequency multiplier.

$Z_{idler}(f)$	Embedding impedance for the idler circuit of a frequency tripler. (Function of frequency.)
$Z_i(f)$	Input embedding impedance. (Function of frequency.)
$Z_o(f)$	Output embedding impedance. (Function of frequency.)
Z_{pi}	Characteristic impedance of a transmission line structure calculated from the knowledge of power flowing through a given cross − section and the current distribution across it.
Z_{pv}	Characteristic impedance of a transmission line structure calculated from the knowledge of power flowing through a given cross − section and the voltage distribution across it.
Z_{vi}	Characteristic impedance of a transmission line structure calculated from the knowledge of current and voltage distribution across a given cross − section.
d_n	Geometric lengths of features on a circuit layout.
e	Base of the natural logarithm, 2.71828182
$e(t)$	Instantaneous value of the voltage − waveform of an input pump signal to a frequency multiplier.
f	Frequency.
f_0	Frequency of the input pump signal to a frequency multiplier.
k	Boltzmann constant, 1.380658×10^{-23} J/K.
n	Multiplication order of a frequency multiplier. For instance, n = 2 for a frequency doubler etc.
q	Electronic charge, $-1.60217733 \times 10^{-19}$ C.
r_a	Radius of the junction contact, or “anode”.

r_{oc}	Inner radius of the ohmic contact.
t	Time.
t_{epi}	Thickness of the epitaxial layer in a diode.
v_e	Average electron drift velocity.
v_{sat}	Average drift saturation velocity of electrons.
$w(V_j)$	Width of the depletion region in a diode. (Function of the potential difference across the junction.)
$\Delta\phi_c(t)$	Instantaneous phase noise in the waveform of the input pump signal to a frequency multiplier.
$\Delta\varphi_v(t)$	Instantaneous phase noise in the waveform of the output signal from a frequency multiplier.
$\Delta a_c(t)$	Instantaneous amplitude noise (fractional) in the input voltage waveform to a frequency multiplier.
$\Delta a_v(t)$	Instantaneous amplitude noise (fractional) in the output voltage waveform from a frequency multiplier.
$\Delta f_c(t)$	Instantaneous frequency deviation of a sinusiodal from its mean value, f_0, due to phase fluctuations/noise.
Γ_{DUT}	Reflection coefficient of a $one-port$ "device under test".
Γ_M	Measured reflection coefficient of a circuit, at a particular port.
$\delta A_c(f)$	Fourier transform of $\Delta a_c(t)$.
$\delta A_v(f)$	Fourier transform of $\Delta a_v(t)$.
$\delta E_l(f)$	Fourier spectrum (lower sideband) of the voltage waveform of the input pump signal to a frequency multiplier. (Function of frequency.)

$\delta E_u(f)$	Fourier spectrum (upper sideband) of the voltage waveform of the input pump signal to a frequency multiplier. (Function of frequency.)
$\delta V_l(f)$	Fourier spectrum (lower sideband) of the output voltage waveform of a frequency multiplier.
$\delta V_u(f)$	Fourier spectrum (upper sideband) of the output voltage waveform of a frequency multiplier.
δ_{buffer}	Skin depth in the buffer layer of a diode.
$\delta\Phi_c(f)$	Fourier transform of $\Delta\phi_{\mathrm{c}}(\mathrm{t})$.
$\delta\Phi_v(f)$	Fourier transform of $\Delta\varphi_{\mathrm{v}}(\mathrm{t})$.
ϵ_s	Dielectric permittivity of GaAs, 13.1.
$\gamma\ (V_j)$	Correction factor used to account for the additional capacitance arising due to the fringing fields at the periphery of a Schottky junction. (Function of the potential difference across the junction.)
μ_e	Electron mobility in a semiconductor.
μ_{epi}	Electron mobility in $\mathrm{n}-$ doped epitaxial layer.
ω	Radial frequency, equivalent to $2\pi\mathrm{f}$.
ω_0	Radial frequency of the input pump signal to a frequency multiplier, equivalent to $2\pi\mathrm{f}_0$.
ϕ	Phase.
ϕ_c	Initial phase of the voltage waveform of an input pump signal. to a frequency multiplier.
ϕ_v	Nonlinear phase term in the output voltage waveform of a frequency multiplier.
π	3.141592654

σ_{buffer}	Conductivity of the buffer layer in a diode.
σ_{epi}	Conductivity of the epitaxial layer in a diode.
φ_v	Total phase of the voltage waveform at the output of a frequency multiplier.

Chapter 1

Introduction

Many physical phenomena can be studied through the measurement of electro-magnetic emissions in the millimeter and submillimeter part of the frequency spectrum. The observation technique employed can be passive whereby the naturally present emissions are simply measured, or active where the target is first illuminated by an appropriate wavelength radiation, and the reflected or transmitted energy is subsequently analyzed.

Applications of the passive technique include, but are not limited to, remote-sensing of the earth's surface from space-based and air-borne platforms, molecular spectroscopy and radio-astronomy. Remote-sensing can be employed to prospect for minerals, estimate the forest and crop cover, study

weather patterns and track climatological changes. Most of these applications revolve around radiometric detection of certain target molecular energy-state transitions, which are in turn related to either emission or absorption lines in the millimeter and sub-millimeter part of the electro-magnetic spectrum. In radio-astronomy, the study of this subtly "encoded" information has revealed, and continues to uncover, vast amounts of knowledge about the formation and evolution of galaxies as well as the compositions of various stars and planets. The past of the universe can be actually "observed" by analyzing the radiation emitted a long time ago (at appropriate red-shifts).

Examples of the active technique can be found in automotive anti-collision systems, in the detection of concealed weapons, in airborne bio-chemical agent detection, in the detection of buried objects, in non-invasive materials testing, in aircraft instrument-landing systems, and in medical imaging. A significant application of the active imaging technique is also found in the estimation of radar cross-sections of various objects via illumination of their (reduced-size) scale models by a submillimeter-wave radar and subsequent measurement of the reflected energy.

1.1 Background and Motivation

The millimeter- and submillimeter-wave radio receivers are predominantly of two types: Direct detector type (like the bolometer) which are useful for applications requiring total power detection, and super-heterodyne type wherein the received radiation is down converted into an intermediate frequency (IF) signal for coherent detection and/or subsequent signal processing. Coherent detection is required for high resolution spectroscopy and

radio interferometry. A key requirement for the operation of such a super-heterodyne receiver is the availability of a local oscillator (LO) signal used to pump a non-linear component such as a low noise superconductor-insulator-superconductor (SIS) junction, a Schottky-diode, or a Hot Electron Bolometer (HEB) device, that down-converts the received signal while preserving its "information" bearing characteristics.

Table-1.1 lists the LO requirements of two millimeter- and submillimeter-wave instruments currently under development: The very high resolution heterodyne spectrometer in a superfluid helium cryostat (HIFI) for the Herschel Space Observatory (HSO) satellite and the ground based Atacama Large Millimeter Array (ALMA) telescope.

Table 1.1: Typical millimeter- and submillimeter-wave LO requirements.

Project	LO Tuning Range (GHz)	Mixer Element	Required LO Power	Notes	Reference
HSO	488 - 546 560 - 633 647 - 710 724 - 793 807 - 848 862 - 953 967 - 1042 1056 - 1113 1127 - 1178 1192 - 1242	SIS & HEB	25 - 50 μW	The need for space-qualification requires extremely reliable, very rugged, compact & light-weight design	[1]
ALMA	27.3 - 33 79 - 94 101 - 104 137 - 151 175 - 199 223 - 263 287 - 358 397 - 488 614 - 708 799 - 938	HFET & SIS	100 μW 15 mW (for the first two lower bands with HFET-type mixers)	Array configuration requires a large number of sources. This implies that the components should be low-cost, moderately reliable, compact & easily reproduceable. LO should be remotely tunable.	[2]

For space-borne applications, the LO system needs to be extremely reliable since there is little possibility of carrying out any repairs subsequent

to the launch of the instrument. Other desirable features include low power consumption, a light weight design, and compact size. Since only a few units need to be produced, cost and ease of assembly are secondary factors. However, for an earth based array telescope receiver, cost and reproduceability are important factors since large numbers of LO systems need to be manufactured. Although the systems are accessible for repairs after commissioning in this case, reliability of the LO system is critical to ensure low "down" times for the telescope considering the large number of LO systems that are deployed.

In the subsequent sections of this chapter, a survey of the existing millimeter- and submillimeter-wave source technology is presented. The fundamental oscillator sources are reviewed first, followed by a brief summary of the current state-of-the-art of millimeter- and submillimter-wave generation via photonic mixing and generation. The final part of the survey presents a comprehensive review of published literature on frequency multipliers spanning the past decade.

1.2 Fundamental Millimeter- and Submillimeter-wave Oscillators

The fundamental millimeter- and submillimeter-wave oscillators may be classified as either tube-type (vacuum or gas-filled) or as solid-state devices. A comprehensive review of the available fundamental oscillator technologies can be found in [3] [4]. An overview of these technologies is presented on the following pages, together with some recent devlopments.

1.2.1 Vacuum and Gas-filled Tube Sources

The most notable sources in this category are the Backward Wave Oscillator (BWO, also known by its trade name: Carcinotron), the Gyrotron, the Traveling Wave Tube Amplifier based oscillator (TWT), the Ledatron (Orotron) and the Magnetron.

Besides being based on "bulky" tubes, all of the above technologies require heavy and bulky support equipment (power supplies, and cooling equipment in some cases) which is an impediment to their use and acceptance. The reliability of vacuum tubes is itself somewhat questionable since the electron gun cathode filament slowly "evaporates" limiting the operational life of the tube. Furthermore, in most cases, the frequency of oscillation is determined by the size of the cavity or the length of the tube. Therefore, frequency tuning of these devices requires some kind of mechanical arrangement to change the size of the resonant cavity. Use of these oscillators as sources for high frequency LO is limited because it is difficult to suitably scale the mechanical structures for such operation.

Nevertheless there is a report of a BWO operating up to 1.2 THz (with 30% tuning band-width, and delivering 1 mW CW RF power) and a Ledatron source generating LO power up to several THz [4].

Although tube-based sources have found widespread application in the laboratory and on air-borne platforms, the weight, size and reliability issues mentioned earlier, have restricted the use of this technology for space applications. Being expensive, this technology is not very suitable for array type receivers either. Consequently, advances in tube technology appear to have leveled off and new sources incorporating tubes are relatively few in number.

Recently however, interest in these technologies has been rekindled due to the implications of rapid advances made in fields as diverse as micro-machining and carbon-nanotube fabrication. These technologies have made it possible to scale the resonant cavities and other associated mechanical structures for operation at higher frequencies, rendering the design and realization of "nano" versions of tube based sources feasible. For instance, a reflex klystron operating at frequencies greater than 300 GHz (and delivering 1 mW of power) [5], a vacuum electron transit time tube source (operating in the terahertz frequency range) employing a micro-machined cold field emitter cathode [6], a micro-fabricated TWT [7], and a 1200 GHz monolithic nanoklystron using carbon-nanotube emitters [8] [9] have all been either demonstrated or proposed. These miniature devices eliminate the bulky support equipment making them attractive as LO sources. However, significant progress needs to be made before viable sources become available based on this approach. The operational life of the novel emitter designs, which are often micro-machined free standing grid structures, remains to be evaluated.

1.2.2 Solid-state Sources

Solid-state oscillators are a reliable and compact alternative to the tube-type fundamental oscillator sources. These can be further classified into two categories: Two-terminal "diode" device based sources, and three-terminal "transistor" device based sources.

Diode based oscillators

The most popular two-terminal devices used in fundamental oscillator sources are the Resonant Tunneling Diode (RTD), the Transferred-Electron Device (TED) commonly known as the Gunn-diode, and the Transit Time Diodes (TDD) such as the IMPact Ionization Avalanche Transit Time (IMPATT) device, the MIxed Tunneling and Avalanche multiplication Transit Time (MITATT) device, the BARrier Injection Transit Time (BARRIT) device and the TUNNEling Transit Time (TUNNETT) diode.

Table-1.2 presents a summary of these two-terminal solid-state devices operating in the fundamental oscillation mode. A good review of this technology is also available in [3] [10].

The RTD is an inherently unstable device due to its negative differential resistance and therefore oscillators based on this device are prone to severe instabilities and bias oscillations. Although receiver systems have been constructed using RTDs [11], use of such devices in practical systems remains fairly uncommon.

The Gunn-diode based oscillators are perhaps the most common solid-state oscillators. These oscillators are low noise, stable, compact, rugged, reliable and can be phase-locked. Besides operating in the fundamental mode (the performance for which is summarized in Table-1.2) these devices are also capable of operating in the second-harmonic mode. When operated in this way, an output power of 3.5 mW at 214 GHz and 1 mW at 315 GHz has been reported [12].

The transit time device based oscillators are inherently extremely noisy and generally not used for sensitive receiver applications.

Table 1.2: Two-terminal solid-state sources, operating in the fundamental mode.

Device Name	Frequency	RF Power	Notes	Ref.	Reference
RTD	360 GHz 712 GHz	3 μW 0.3 μW	Low Noise, Unstable	[14]	Brown 1991
TED Gunn-diode	103 GHz 132 GHz 152 GHz 162 GHz	200 mW 130 mW 80 mW 25 mW	Low Noise	[15] [16]	Eisele 1998, 1995
	106 GHz 136 GHz 152 GHz	300 mW 130 mW 125 mW	With power combining, Low Noise		
	40 - 300 GHz	500 - 1 mW	Low Noise	[10]	Eisele 1999
TTD Si-IMPATT	285 GHz 301 GHz 361 GHz	7.5 mW 1.2 mW 0.2 mW	Very Noisy	[17]	Ino 1976
	60 - 361 GHz	2000 - 0.2 mW	Very Noisy	[10]	Eisele 1999
TTD GaAs-IMPATT	33 - 160 GHz	3000 - 20 mW	Very Noisy		
TTD Si-MITATT	100 GHz	25 mW	Very Noisy		
TTD GaAs-MITATT	140 GHz	7 mW	Very Noisy		
TDD Si-BARITT	40 - 60 GHz	3.8 - 1 mW	Very Noisy		
TTD GaAs-TUNNETT	100 - 107 GHz	105 - 95 mW	Noisier than TED	[18]	Eisele 1998

Like the Gunn-diode based counterparts, the TUNNETT based oscillators can also be designed to operate in the second-harmonic mode. Designs using this mode of operation have been reported to produce an output power of 10 mW at 202 GHz and 4 mW at 235 GHz [13].

Transistor based oscillators

The most common three-terminal devices used in fundamental oscillator sources are the Hetero-junction Bipolar Transistor (HBT), the High Electron Mobility Transistor (HEMT), the Pseudomorphic HEMT (or PHEMT), and the doped channel Psudomorphic Heterostructure Field Effect Transistor (or

PHFET). Table-1.3 presents a summary of the current oscillator technology based on these three-terminal devices.

Table 1.3: Three-terminal solid-state fundamental oscillator sources.

Device Name	Highest Operating Frequency	RF Power	Notes	Ref.	Reference
HBT	73.5 GHz	93 mW	InGaP/GaAs	[19]	Heins 1999
HEMT	76 - 77 GHz	7 dBm	DRO-stabilized	[20]	Siweris 1999
PHEMT	77 GHz	300 μW	Low-noise	[21]	Vaughan 1996
PHFET	94 GHz	6 mW	On chip buffer Amp.	[22]	Bangert 1994

A comparison of this summary with the one provided in [3] (which was prepared in the early 1990s) reveals that there are no significant improvements in the maximum operating frequencies of these devices over the past decade despite significant research effort. Most of the research effort appears to be aimed at designing increasingly complex circuits and integrating more receiver functions into a single chip, rather than improving the underlying oscillator device technology. The HEMT-HBT integration technology, which enables the designer to integrate oscillators and amplifiers into a single chip and increase the available output power, is a result of such efforts. Clearly this approach is limited by the underlying device physics and would need significant breakthrough in semiconductor research before being useful for generating LO power at frequencies much above the 100–200 GHz frequency range.

1.3 Millimeter- and Submillimeter-wave Generation by Photonic Mixing and Detection

Another relatively recent development is the generation of LO power by photonic mixing. Under this approach, LO power is generated by mixing two locked lasers with a difference frequency equal to the desired LO frequency and detecting the beat-note. This technique holds great advantages over conventional LO sources especially for multi-band receiver systems. The difference frequency between the lasers could easily be made to span the entire millimeter- and submillimeter-wave spectrum and beyond. This would enable the design (at least in principle) of a single LO source capable of tuning over the entire band of interest, and eliminating banks of conventional LO sources required to accomplish the same task.

The two critical components required to make such an approach feasible are: a laser source and a photo-detector. The laser source technology is fairly mature and inexpensive solid-state lasers meeting the requirements are currently available. The same cannot be said for the photo-detector technology. Photo-detectors generally consist of a semiconductor material possessing certain band-gap energy that makes them sensitive to light (photons) of a certain wavelength. Photons of light cause generation of electron-hole pairs which under the influence of an externally applied electric field constitute the detected current. Typical commercial photo-detectors fail to respond faster than about 50 GHz since the devices are too long for the carriers generated by incident light to travel to the device terminals. The device capacitance

also adversely affects the high frequency performance of such devices. Considerable research effort is ongoing at the present time to overcome these shortcomings.

One approach is to tailor the device junction with a doping profile that permits carriers to travel at overshoot velocities over small distances, thereby achieving faster devices with a useful high frequency response. Another technique aimed at improving the "detection efficiency" (and thus increasing the LO power generated), involves using traveling-wave or velocity matched devices. In a traveling wave photo-mixer, the active area is elongated in one dimension and the output currents are collected on to a traveling-wave structure such as a coplanar waveguide. In a velocity matched device [23], the output from several high-speed photo-detectors is combined coherently.

Plenty of published results [2], [24]-[32] can be found demonstrating generation of LO power using this technique. However owing to the constraints mentioned earlier, the maximum frequency is limited to about 100 GHz. [24] represents the state-of-the-art of photonic LO generation with 0.5 mW reported at 120 GHz, although an output power of 10 μW has been reported as high as 200 GHz recently. Reports of smaller photomixing power outputs up to 3.8 THz can be found [27].

To optimize the use of whatever little power is generated at higher frequencies, receivers that have a photo-mixer integrated with the low-noise SIS frequency down converting junction have been built. Using this technique, a receiver with noise temperature of 331K has been reported at 630 GHz [32].

Despite these recent advances, the photo-detector technology is not mature enough to deliver a practical photonic LO for frequencies beyond the

100–200 GHz range. Significant progress needs to be made before this approach becomes capable of yielding a viable submillimeter-wave LO source. The sideband noise in the LO generated by photonic mixing is also of major concern in sensitive receiver applications [33].

Based on the preceding review of the current state-of-the-art of fundamental LO design, it is obvious that the only viable approach to realizing compact, light-weight, low-noise and reliable LO systems above 100–200 GHz appears to be a frequency multiplier (or a cascade of frequency multipliers) pumped by a lower frequency fundamental oscillator source, such as a Gunn-diode based oscillator. The state-of-the-art with respect to frequency multiplier technology is presented in the following section. This will help identify problem areas and establish a clear direction for the present research.

1.4 Millimeter- and Submillimeter-wave Frequency Multipliers

A complete description of the current state of the millimeter- and submillimter-wave frequency multiplier technology is presented in Appendix-A, so only a brief summary of the current state-of-the-art is given in this section. Table-1.4 gives a list of the types of frequency multipliers in use today for the generation of LO power up to about 2.5 THz.

The abrupt junction Schottky diode as a discrete planar device and as a planar monolithic device forms the most dominant technology for generation of microwave power. Its use is prevalent in various configurations such as a single diode, balanced and un-balanced multiple diode-arrays, and as

Table 1.4: Categorization of frequency multiplier technologies.

Symbol	Description of Configuration
F	FET/MESFET/HFET/HJFET in a hybrid microwave int. circuit (MIC) or monolithic microwave int. circuit (MMIC)
T	Hetero-junction barrier transistor incorporated into a hybrid MIC or MMIC
M	HEMT/PHEMT/RTHEMT incorporated into a hybrid MIC or MMIC
Mb	Balanced config. of HEMT/PHEMT/RTHEMT incorporated into a hybrid MIC or MMIC
S	Whisker contacted abrupt-junction Schottky diode in waveguide
sS	Abrupt-junction Schottky diode incorporated into a planar hybrid MIC
mS	Abrupt-junction Schottky diode incorporated into a planar MMIC
Sb	Balanced config. of planar abrupt-junction Schottky diodes in waveguide
sSb	Balanced config. of abrupt-junction Schottky diodes incorporated into a planar hybrid MIC
pS	Planar abrupt-junction Schottky diode in waveguide
pSb	Balanced config. of planar abrupt-junction Schottky diodes in waveguide
mSb	Balanced config. of abrupt-junction Schottky diodes incorporated into a planar MMIC
SG	Planar matrix of planar abrupt-junction diodes
QG	Planar matrix of quantum-well diodes
SGb	Planar matrix of a balanced config. of abrupt-junction diodes
NL	Non-linear transmission line, includes planar solitons
Q	Whisker contacted quantum-well diode in waveguide
sQ	Quantum-well diode incorporated into a planar hybrid MIC
mQ	Quantum-well diode incorporated into a planar MMIC
sD	Step-recovery diode incorporated into a planar hybrid MIC
pH	Planar hetero-junction barrier varactor diode in waveguide
sH	Hetero-junction barrier varactor diode incorporated into a planar hybrid MIC

diode grids. Other devices in use include the Hetero-junction Barrier Varactor (HBV), the Quantum Well Diode as well well as three-terminal devices like the Hetero-junction Barrier Transistor (HBT), the High Electron Mobility Transistor (HEMT) and their variants. Reports on distributed element frequency multiplier technologies such as transmission lines loaded with multiple Schottky diodes or HBVs as well as soliton generators, though rare, can be found.

The most important characteristic of a multiplier for any particular frequency is the amount of its output power. The plots on the following pages show the output power versus frequency for more than 100 multipliers reviewed in Appendix-A. Only *experimentally measured power* is plotted al-

though no qualifications are made regarding the power measurement and calibration techniques. A summary of the existing frequency multiplier technologies is provided in Table-1.5 and 1.6.

Table 1.5: Summary of the existing frequency multiplier technologies.

Technology	Symbol	Number	Mount Type	Output Frequency Range	Advantages	Disadvantages
Abrupt-Junction Schottky	S	1 - 4	W/G Quasi-optic	16 - 750 GHz	• High frequency of operation	◦ Mechanically poor ◦ Difficult to assemble
	pS	1	W/G	50 - 480 GHz	• High frequency of operation • Integrated contact makes assembly easier	
	Sb	2	W/G	800 GHz	• High frequency of operation	◦ Mechanically poor ◦ Difficult to assemble ◦ Matched pair of diodes required
	sS	1	Hybrid MIC Quasi-optic	16 - 600 GHz	• Easier to assemble than S or Sb • Rugged • Little or no mechanical tuning	◦ Assembly variation is difficult to model ◦ Scaling up in frequency is not straightforward
	sSb	2 - 6	Hybrid MIC	7.2 - 220 GHz	• Easier to assemble than S or Sb • Rugged • Little or no mechanical tuning	◦ Assembly variation is difficult to model ◦ Scaling up in frequency is not straightforward ◦ Matched pair of diodes required
	mS	1 - 2	MMIC	5.6 - 320 GHz	• Very rugged • Monolithic fab. • Easiest to assemble • Min. mechanical tuning • Scalable designs	◦ THz designs need extremely thin substrates. Heat dissipation could be a problem
	mSb	2, 4	MMIC	36 - 2550 GHz		
	SG	Up to 1000s	Planar quasi-optic grid	10 - 1000 GHz	• High output power • Little or no mechanical tuning	◦ Fab. yield is low ◦ Quasi-optical

Table 1.6: Summary of the existing frequency multiplier technologies (continued).

Technology	Symbol	Number	Mount Type	Output Frequency Range	Advantages	Disadvantages
HBV	sH		Hybrid MIC Micro-strip	26.5 - 40 GHz	• Idler circuit eliminated	◦ Most designs need mechanical tuners ◦ Narrow band-width ◦ Epitaxial stacks have heat dissipation problems
	pH		W/G MMIC	26.5 - 290 GHz		
Quantum Well	Q		W/G	90 - 190 GHz		◦ Low power and efficiency
	sQ		Hybrid MIC	60 - 90 GHz		
	mQ	1	MMIC	210 GHz		
	QG	1300	Planar quasi-optic grid	99 GHz		
Step recovery diode	SD	1	Hybrid MIC	10 GHz		◦ Low frequency of operation
HEMT/ PHEMT/ RTHEMT	M	1 - 2	MMIC	1.4 - 180 GHz	• System on chip designs possible	◦ Suppressing unwanted harmonics a design issue ◦ Active devices limit max. frequency
	Mb	4	MMIC	42 - 300 GHz		
HBT	T		MMIC	54.5 GHz		
FET/ MESFET/ HFET/ HJFET	F		MMIC	24 - 96 GHz		
Non-linear trans. line	NL	8 - 20	Hybrid MIC and MMIC	26 - 130 GHz	• Rugged • Wide band-width • No tuning needed	◦ Fabrication and assembly is difficult ◦ Low power and efficiency

From the plots in Figure-1.1, 1.2, and 1.3 as well as the summary presented in Table-1.5 and 1.6, a number of inferences can be made regarding the state-of-the-art of frequency multiplier technology.

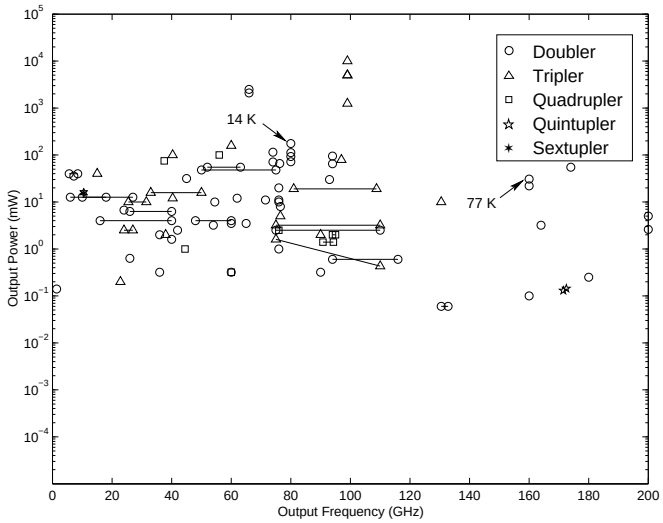

Figure 1.1: State-of-the-art frequency multiplier performance survey (1991–2001): Output power versus frequency up to 200 GHz. See Appendix-A.

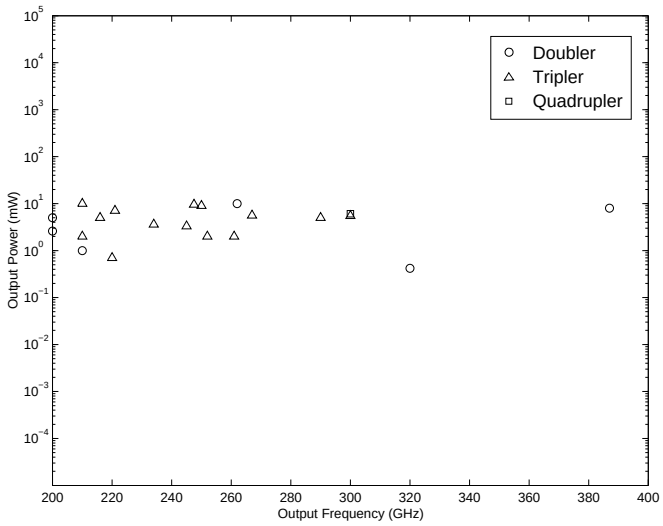

Figure 1.2: State-of-the-art frequency multiplier performance survey (1991–2001): Output power versus frequency from 200 GHz to 400 GHz. See Appendix-A.

Several choices exist for multipliers with an output frequencies up to 100 GHz. For low power applications, active integrated (MMIC) designs based

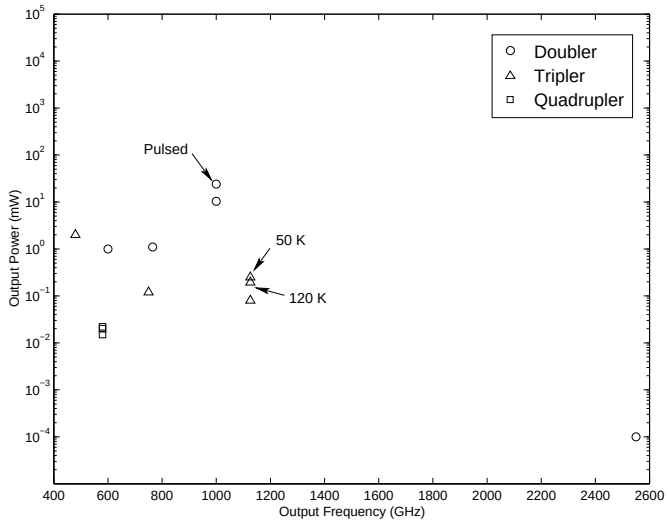

Figure 1.3: State-of-the-art frequency multiplier performance survey (1991–2001): Output power versus frequency from 400 GHz to 2600 GHz. See Appendix-A.

on FET, HEMT or HBT technology are feasible. These have an advantage since they allow integration of several receiver functions into a single chip. However due to the small feature size, such designs are not suitable for generating high output power. For high power requirement (more than a few tens of milliwatts), discrete planar abrupt-junction Schottky diode arrays incorporated into planar circuits ("hybrid" MIC type frequency multipliers) are prevalent. The fairly large size of these devices makes such multipliers easy to assemble. Their reliability has rendered the older whisker contacted Schottky diode designs obsolete.

For the 100–300 GHz frequency range, HEMT is the only suitable technology for realizing active MMIC frequency multipliers. At these frequencies, the discrete planar diode on substrate (hybrid-MIC) approach becomes questionable due to the reduced size of the device and the associated design

uncertainty and assembly problems. However Schottky diode based MMIC multipliers have been demonstrated to be effective for this range of frequencies. Some "integrated whisker" designs are also found in this frequency range. Again, the push to move away from traditional whisker contacted designs, is nearly complete.

For frequencies above about 400 GHz, the abrupt junction Schottky-diode is the only practical device with demonstrated operation. The size of the devices for this frequencies, makes it impractical to try hybrid designs, and a fully integrated monolithic approach appears to be the only viable solution. Multipliers designed using this approach have demonstrated LO power generation up to 2.5 THz.

Other esoteric devices have found limited applications. Devices such as the Hetero-junction Barrier Varactor and the asymmetrically doped back-to-back Schottky diode eliminate the need for the design of idler circuits in frequency tripler applications, but have limited output power and bandwidth. Some niche applications have seen the use of quantum well diodes. However despite significant research, little improvements in power or frequency coverage have emerged for these devices for quite some time.

1.5 Research Objectives

Based on the foregoing discussion in Section-1.4, it is evident that Schottky diode based MIC and MMIC frequency multipliers should continue to be the dominant LO sources for the foreseeable future. The first part of the research presented in this dissertation primarily dealt with an effort to extend the current hybrid-MIC frequency multiplier technology to cover the 100–300

GHz frequency range. The limitations of the approach, uncovered as a result of this effort, are presented. The second part of the research focused on extending the MMIC technology for designing and implementing frequency multipliers in this frequency range.

In Chapter-2, the design, implementation, and evaluation of two tuner-less hybrid-MIC type frequency doublers, based on abrupt-junction Schottky diodes, are presented. The limitations of using this approach is investigated by reviewing the shortcomings of these designs, and a case made for planar monolithic type frequency multiplier design.

Chapter-3 describes an investigation into the demands placed by the requirements of frequency multiplier design on planar monolithic technology. Appropriate existing fabrication technologies have been identified, and extended where required, to make such a design feasible.

Chapter-4 presents the design, implementation, and evaluation of a performance optimized, tuner-less, monolithic frequency tripler based on the circuit elements and topologies developed and presented in Chapter-3. Comparison between the simulated and actual performance is made and factors limiting the operational efficiency and bandwidth of the design identified.

With ever increasing receiver sensitivities, the LO noise (both amplitude and phase) is a cause for significant concern. Chapter-5 presents the results of a study performed to quantify the input to output noise transfer characteristics of a simple single diode frequency doubler. These results could be used to predict the amount of noise generated at the multiplier output for a given noise present in the input pump source.

Finally, the above research is summarized in Chapter-6 by listing the important contributions of this work and by suggesting a path for future study.

Chapter 2

Hybrid-MIC Frequency Doublers

A 55/110 GHz frequency doubler and a 110/220 GHz frequency doubler were designed, fabricated, and evaluated. Both the designs were based on discrete planar diode arrays. In each case, the diode array was incorporated into a planar circuit fabricated on fused-quartz substrate to yield a "hybrid" MIC type frequency doubler. Details of the these doublers are presented in this chapter. The 55/110 GHz version is discussed first. The 110/220 GHz version was very similar and is summarized towards the end of this chapter.

Both the doublers were based on the configuration of the 40/80 GHz frequency doubler presented in [137], however the details of the embedding networks employed in the new designs were different from those used in the 40/80 GHz frequency doubler. The goal behind this effort was to gain familiarity with the process of designing frequency doublers and to learn the operation of various simulation tools used for the purpose. This knowledge would be crucial for the later part of this research. Study of the development process of the hybrid-MIC frequency doublers was also expected to expose the limitations of this technology for high frequency multiplier work, and thus set a stage for an investigation of the monolithic approach.

2.1 Introduction

A frequency doubler is a device with two RF ports. The input port is driven (or "pumped") by a source or generator at some frequency f_0, while the second harmonic of the source (at frequency $2f_0$) is available from the output port. The doubling of frequency is brought about by the action of a non-linear device(s) present in the circuit. The conversion efficiency of the frequency doubler, η_m, depends on several factors: The input and output embedding impedance presented to the non-linear device(s), the losses inherent in the non-linear device(s), and the losses in the input and output coupling networks. If the non-linear device(s) were lossless (such as a lossless varactor), then in the absence of any circuit losses it would be possible to achieve a conversion efficiency of 100% [138] [139] provided the input and output embedding impedances were optimally designed. Of course real world frequency doublers have device and circuit losses which tend to lower the actual realized efficiency.

Since the operation of a frequency doubler is based on a non-linear phenomena, the optimal input and output embedding impedances are a function of the input pump power. In general, a frequency doubler should be expected to operate close to its peak efficiency only when pumped by an input power level close to the design value. For other input power levels, the optimum input and output embedding impedances depart from the ones present in the frequency doubler circuit and consequently, the efficiency of conversion drops.

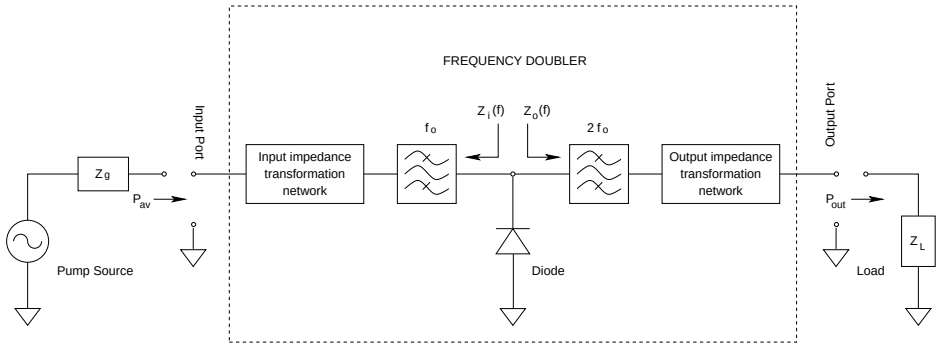

Figure 2.1: A single diode based frequency doubler.

Figure-2.1 illustrates the circuit configuration of a typical frequency doubler designed around a single diode. The input impedance matching network serves to transform the generator (source) impedance to the optimum input embedding impedance required to be presented to the diode. The output impedance matching network serves a similar purpose at the output frequency, transforming the load impedance into a value that optimizes the conversion efficiency (i.e. optimum output embedding impedance). The input and output filters serve to isolate the input and output ports, preventing the possibility of the input power propagating into the output port and vice-versa. Since the equivalent impedance, $Z_{emb}(f)$, presented across the diode

terminals is a parallel combination of $Z_i(f)$ and $Z_o(f)$, the filters should be designed such that $Z_i(2f_0)$ and $Z_o(f_0)$ are as close to an open circuit as possible. This prevents the output network from shorting out the input pump power or the input network from shunting the second harmonic signal (which represents the useful output of the frequency doubler).

2.2 Balanced Frequency Doubler Configuration

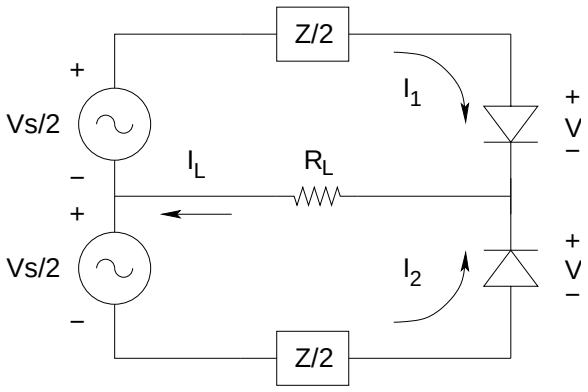

Figure 2.2: An alternate doubler circuit employing a balanced diode configuration.

Figure-2.2 shows an alternate arrangement of varactor diodes that could be employed in frequency doubler designs instead of the "single-ended" diode configuration described in the previous section. The operation of such a configuration as a frequency doubler can be described as follows: The non-linear charge-voltage relationship for each of the two varactors may be represented by a power-series

$$Q(V) = a_1V + a_2V^2 + a_3V^3 + a_4V^4 + \ldots \tag{2.1}$$

where V is the voltage across the diode and $Q(V)$ is the corresponding charge stored in the device. The current through the diode can be computed from

$$I = \frac{dQ}{dt} = [a_1 + 2a_2V + 3a_3V^2 + 4a_4V^3 + \ldots]\frac{dV}{dt} \tag{2.2}$$

Thus for a voltage $V(t)$ across the diodes given by

$$V(t) = sin(k\omega_0 t) \tag{2.3}$$

the currents $I_1(t)$, $I_2(t)$ in the two loops of the circuit take the form,

$$I_1(t) = b_1 cos(k\omega_0 t) + b_2 sin(2k\omega_0 t) + b_3 cos(3k\omega_0 t) + \ldots \tag{2.4}$$

$$I_2(t) = -b_1 cos(k\omega_0 t) + b_2 sin(2k\omega_0 t) - b_3 cos(3k\omega_0 t) + \ldots \tag{2.5}$$

Consequently the load current, I_L, through R_L becomes

$$I_L(t) = I_1(t) + I_2(t) = c_2 sin(2k\omega_0 t) + c_4 sin(4k\omega_0 t) + \ldots \tag{2.6}$$

which shows that only even harmonic currents flow in the load circuit. Therefore a circuit configuration consisting of anti-series arrangement of diodes placed at a junction of balanced and unbalanced transmission lines could operate as a frequency doubler. Furthermore, if the incident pump power on the diodes at frequency f_0 were in a balanced mode, then the generated output power at frequency $2f_0$ would be in the unbalanced mode. If the unbalanced line were to be designed so as not to support a balanced mode at the input frequency, then input-output isolation could be achieved without the use of filters as was necessary in the case of the doubler employing a single diode. Figure-2.3 shows one possible arrangement that is based on this configuration and was employed to realize the frequency doublers for the purpose of this study. Its operation as a 55/110 GHz frequency doubler is described in the next section.

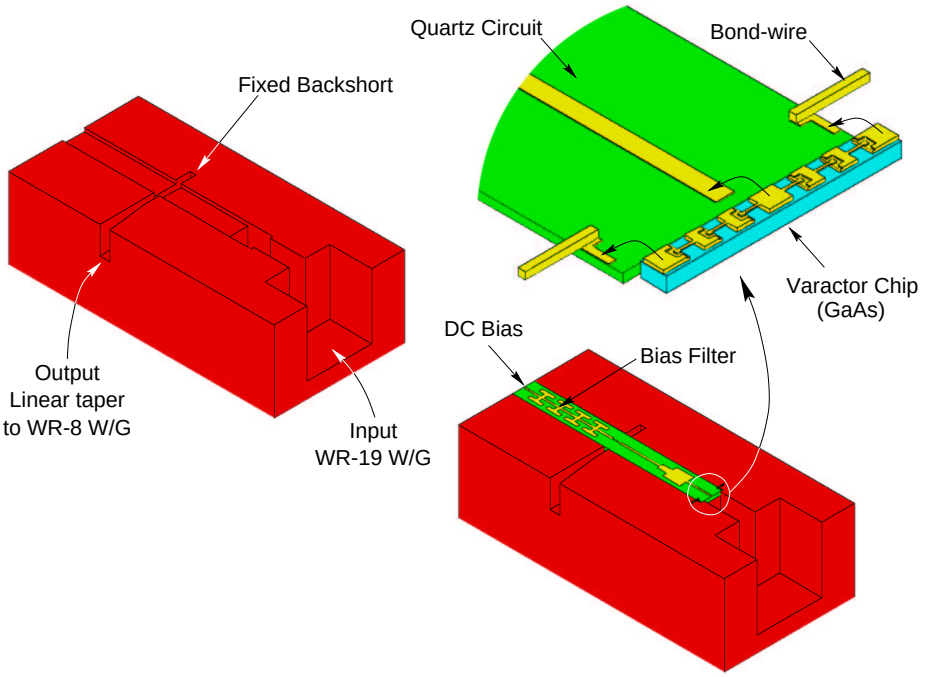

Figure 2.3: The 55/100 GHz frequency doubler. Figure shows a cut-away view of the doubler mount revealing the location of the planar quartz circuit and the placement of the diode array on it.

2.3 Operation of the Doubler Circuit

The input of the frequency doubler was a WR-19 (U-Band) rectangular waveguide, that provided the incident pump power to the diode array. The dominant TE_{10} mode in the input waveguide ensured that the incident power was in the balanced mode as desired for circuit operation. The output network, which was a planar circuit on a 5 mil fused-quartz substrate, consisted of a "quasi-coaxial" line cascaded to a microstrip transmission line and served to couple the second harmonic power out of the diode array in an unbalanced mode. The cross section of the output network was designed to have dimensions such that it did not support signal propagation at the input frequency.

The second harmonic power generated by the diode array could, in principle, propagate into the WR-19 input waveguide as an unbalanced TM_{11} mode. To prevent this, the height of the input waveguide was reduced to a quarter of the full height near the location of the diodes. This modification ensured that the TM_{11} mode was cut-off, thereby preventing the propagation of any second harmonic power towards the input port. The length of the reduced height section was ensured to be long enough to cause sufficient attenuation of the "evanescent" TM_{11} mode. It also served as a design variable to achieve a good input impedance match. Power was coupled out from the microstrip line into a reduced height section (a fifth of the full waveguide height) of the output waveguide through an appropriately designed probe coupling arrangement that included a fixed back-short. The reduced height waveguide had a linear taper to full height WR-8 (F-band) waveguide that formed the output flange. The various microstrip transmission line segments with differing characteristic impedances served as impedance transforming sections to match the waveguide probe to the diode array. The "hammer-head" filter structure seen beyond the cross output waveguide was simply a low-pass DC filter arrangement enabling the application of DC bias to the varactor diodes, via the microstrip metalization, without sacrificing any second harmonic power to the DC bias network.

The diode array comprised of two 3-diodes-in-series sections arranged in an anti-series configuration. The design of this planar discrete array is discussed next.

2.4 Planar Schottky Varactor Design

In this section, the Schottky varactor theory is briefly reviewed followed by its application to set the primary design parameters for the planar varactor chip. Finally, the analysis to obtain the specification and design for the planar discrete diode array is presented.

2.4.1 Review of the Schottky Varactor Theory

A Schottky junction is created by the deposition of metal (such as Platinum or Titanium) on the surface of an appropriate semi-conducting material (such as n-doped GaAs). The non-linear behavior is due to the energy barrier set up at such a metal-semiconductor junction. Figure-2.4 shows a typical GaAs Schottky diode in planarized form. The semi-conducting side of the junction is composed of a thin "epitaxial layer" on top of a relatively thicker (and more heavily doped) "buffer layer". The entire structure rests on top of a semi-insulating GaAs substrate which provides mechanical support but does not contribute to the fundamental operation of the device. The electrical contact to the buffer layer is provided through an "ohmic" pad which is also a metal-semiconductor interface directly on the buffer layer. Since the buffer layer is heavily doped, the energy barrier created is very thin and the electrons can flow in a bi-directional manner due to the tunneling mechanism that dominates the operation of such a junction.

In Schottky diodes used for millimeter- and submillimeter-wave frequency multiplier work, the typical buffer layer doping is about $5 \times 10^{18}\ cm^{-3}$ to ensure good ohmic contacts and low "bulk resistance". Typical epitaxial layer doping levels range from $1 \times 10^{16}\ cm^{-3}$ to $8 \times 10^{17}\ cm^{-3}$.

Although the semi-insulating GaAs does not contribute to the fundamental operation of the diode, it does limit its performance by enhancing

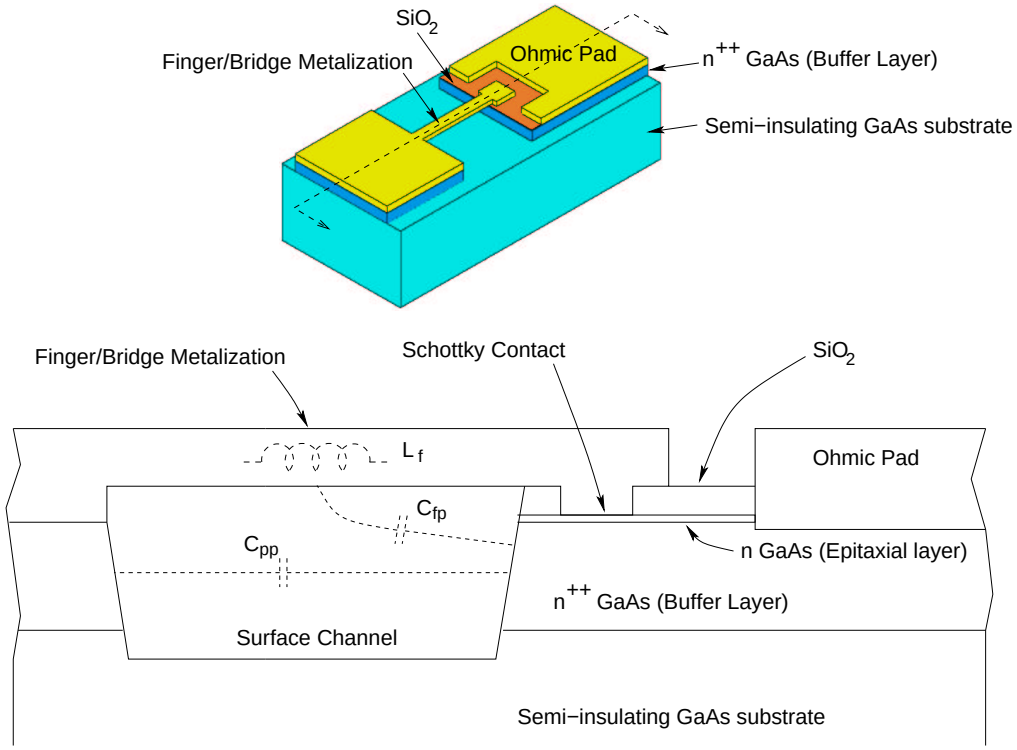

Figure 2.4: Details of a planar Schottky varactor.

certain parasitic capacitances (shown marked in Figure-2.4) associated with the device geometry. The semi-insulating material present under the contact bridge metalization and the proximity of the Schottky contact is most detrimental to the performance of the diode. Consequently, it is removed from these regions as shown in the figure. See [140] for a detailed treatment of this topic.

I-V Characteristic

The conduction current through a Schottky junction is related to the voltage across the junction by the equation

$$I(V_j) = I_0(e^{\frac{qV_j}{kT}} - 1) \tag{2.7}$$

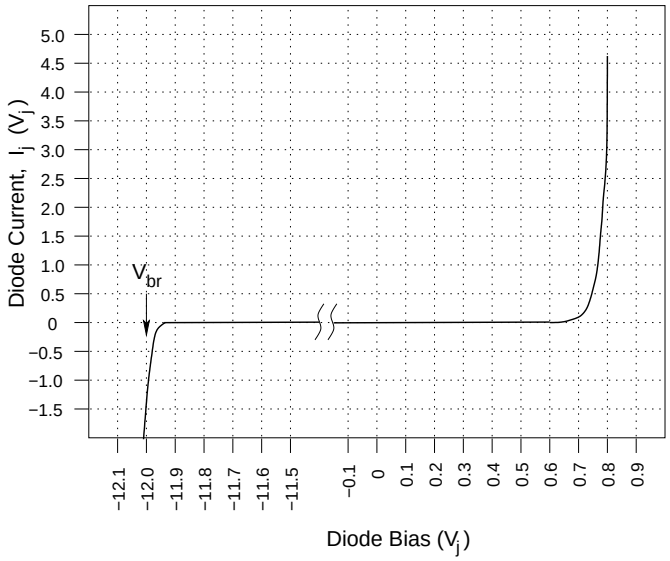

Figure 2.5: Typical Current-Voltage relationship for a Schottky varactor.

where V_j is the voltage across the Schottky contact, and I_0 is the reverse saturation current. Of course, the relation is only valid for reverse bias voltages that do not exceed the reverse breakdown voltage, V_{br}, for the diode (explained later). The voltage across the terminals of the physical diode, V_d, may be computed by adding the voltage drop occurring in the parasitic series resistance of the device. Therefore

$$V_d = V_j + I(V_j)R_s \tag{2.8}$$

where R_s represents the total parasitic series resistance. The typical current-voltage relationship for a GaAs Schottky diode is illustrated in Figure-2.5.

Reverse Breakdown Voltage

The reverse breakdown voltage, V_{br}, of a diode is defined as the minimum reverse bias that causes the diode current to exceed a certain preselected minimum value such as 1 μA or 1 mA. Although referred to as "breakdown", the

large reverse current when the reverse bias exceeds this value is a completely reversible process and does not damage the diode in any way. However, there is a limit to the maximum reverse current in the diode. The heat dissipated in the diode causes a rise in temperature, which if unchecked, could lead to thermal deterioration of the device. This places an upper limit on the maximum reverse bias that can be applied on a diode.

The mechanisms responsible for the reverse current are: thermal instabilities, tunneling and avalanche breakdown. For the doping levels used in practical diodes, the later is the dominant mechanism. Typically, diodes with a low level of epitaxial layer doping exhibit higher reverse breakdown voltages than those with higher levels of epitaxial layer doping. The expected breakdown voltages of a GaAs based planar p^+-n junction as a function of the non-degenerate side (epitaxial) doping are given in [141] and are reproduced in Figure-2.6. These are also applicable to the GaAs-metal Schottky contact diodes.

Junction Capacitance

The non-linear junction capacitance, $C_j(V_j)$, is the result of charge separation across the depletion region created by the application of a reverse bias voltage. Since the depletion region width is dependent on the magnitude of the bias voltage, so is the resulting junction capacitance. For the abrupt junction case the depletion region width $w(V_j)$ is given by

$$w(V_j) = \left[\frac{2\epsilon_s(V_{bi} - V_j)}{qN_d}\right]^{\frac{1}{2}} \tag{2.9}$$

where V_j is the voltage across the junction, V_{bi} is the built-in junction potential, ϵ_s is the dielectric permittivity of GaAs, and N_d is the epitaxial layer

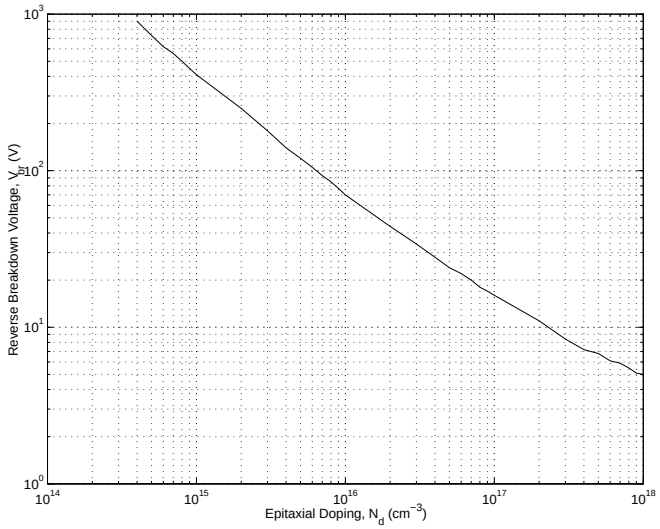

Figure 2.6: Reverse breakdown voltages as a function of epitaxial layer doping level.

doping. If the cross-sectional area of the diode is A, then the charge displaced out of the depletion region, $Q(V_j)$, may be computed from

$$Q(V_j) = qN_dAw(V_j) = \sqrt{2qN_dA\epsilon_s(V_{bi} - V_j)} \tag{2.10}$$

The capacitance may be computed by considering the junction to be a parallel plate capacitor with a plate separation of $w(V_j)$ and with plate area A. Thus the voltage dependent junction capacitance, $C_j(V_j)$, may be written as

$$C_j(V_j) = \frac{\epsilon_s A}{w(V_j)} = A\left[\frac{qN_d\epsilon_s}{2(V_{bi} - V_j)}\right]^{\frac{1}{2}} \tag{2.11}$$

A voltage dependent correction factor, $\gamma(V_j)$, can be used to correct for the effects of fringing fields [142] at the periphery of the epitaxial layer. The corrected $C_j(V_j)$ then becomes

$$C_j(V_j) = A\gamma(V_j)\left[\frac{qN_d\epsilon_s}{2(V_{bi} - V_j)}\right]^{\frac{1}{2}} \tag{2.12}$$

This treatment assumes that the charge is confined in an infinitesimally thin sheet in the epitaxial layer at the end of the depletion region. In reality, the charge spreads out to a small distance in the epitaxial layer. Nevertheless, the capacitance as estimated from Equation-2.12 is fairly accurate for all cases except when $V_j = V_{bi}$. The charge distribution in the epitaxial layer becomes significant under conditions close to flat-band bias. The junction capacitance is observed to peak for a junction voltage slightly less than the flat-band voltage. However since varactor multipliers are operated with the diodes sufficiently reverse biased, this departure turns out to be of little consequence. Figure-2.7 shows typical C-V characteristic for an abrupt junction Schottky diode varactor, under reverse bias.

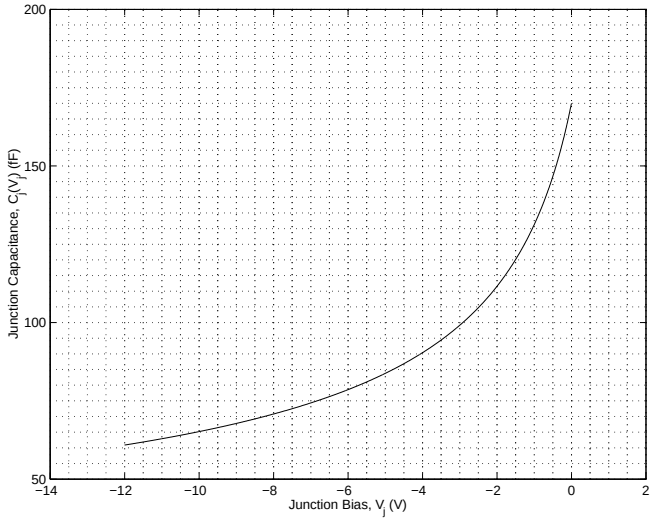

Figure 2.7: Typical variation of the varactor junction capacitance with an applied (reverse) bias voltage.

Series Resistance

The parasitic series resistance, R_s, associated with the diode geometry of Figure-2.4 is comprised of several components: resistance of the un-depleted epitaxial layer (R_{epi}), the spreading resistance arising out of ohmic losses in the buffer layer below the anode as the vertical column of current spreads out into the bulk of the buffer (R_{spread}), the resistance of the buffer layer (R_{buffer}), and the resistance of the ohmic contact (R_{ohmic}). Since all these components occur in series, the total parasitic series resistance may be obtained by summing all the components

$$R_s = R_{epi} + R_{spread} + R_{buffer} + R_{ohmic} \tag{2.13}$$

The width of the un-depleted epitaxial layer is a non-linear function of the applied junction bias as per Equation-2.9. Consequently, the resistance of the un-depleted epitaxial layer has non-linear dependence on the applied bias as well. However in practical cases the variation is small and the use of the maximum value for R_{epi}, corresponding to full epitaxial layer thickness, is justified. This can be computed from

$$R_{epi} = \frac{t_{epi}}{\sigma_{epi} A} \tag{2.14}$$

where t_{epi} is the thickness of the epitaxial layer and σ_{epi}, its conductivity. The conductivity can be computed from the electron mobility, μ_{epi}, using the standard relation

$$\sigma_{epi} = q\mu_{epi} N_d \tag{2.15}$$

Substitution of the equation for σ_{epi} into the expression for R_{epi} yields

$$R_{epi} = \frac{t_{epi}}{qA\mu_{epi} N_d} \tag{2.16}$$

To minimize R_{epi}, the thickness of the epitaxial layer should be chosen to be as small as possible but larger than the maximum depletion region width to avoid punch-through.

The spreading resistance, R_{spread}, may be computed using the relation given by [143] [144]

$$R_{spread} = \frac{1}{4\pi\delta_{buffer}\sigma_{buffer}} \tag{2.17}$$

where δ_{buffer} is the skin depth in the buffer layer given by

$$\delta_{buffer} = \frac{1}{\sqrt{\pi f \mu_0 \sigma_{buffer}}} \tag{2.18}$$

σ_{buffer} might be computed from the knowledge of the mobility, μ_{buffer}, and doping, N_{buffer}, of the buffer layer using

$$\sigma_{buffer} = q\mu_{buffer}N_{buffer} \tag{2.19}$$

The resistance of the buffer layer in the semi-cylindrical region enclosed between the outer radius of the anode and the inner radius of the ohmic contact can be computed from

$$R_{buffer} = \frac{1}{2\pi\delta_{buffer}\sigma_{buffer}} ln\left(\frac{r_{oc}}{r_a}\right) \tag{2.20}$$

If the thickness of the buffer, t_{buffer}, is less than δ_{buffer} at the operating frequency, f, then t_{buffer} should be used instead of δ_{buffer} in computing R_{spread} and R_{buffer} using Equations-2.17 and 2.20 respectively.

The last term in Equation-2.13, R_{ohmic}, which represents the ohmic contact resistance is generally very small compared to the other parasitic resistance components described thus far, and can usually be ignored. The large size of the ohmic contacts in the planar diode array used in this study further ensured a small magnitude of the ohmic contact resistance.

An equivalent circuit model of a planar realization of a Schottky diode incorporating the junction capacitance and all of the parasitic resistive, inductive and capacitive components is presented in Figure-2.8.

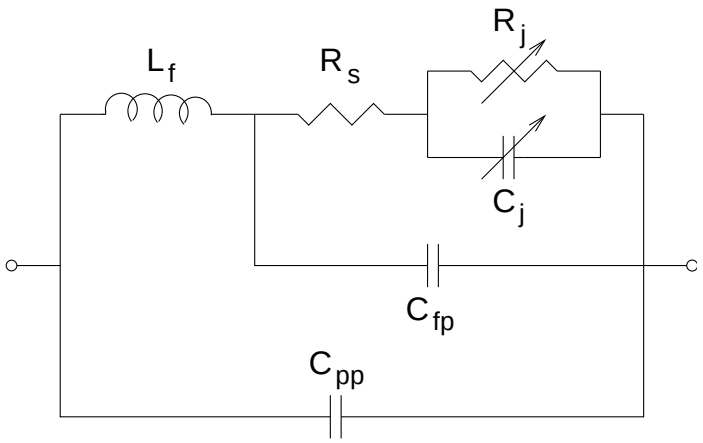

Figure 2.8: Equivalent circuit model of a Schottky junction varactor diode.

2.4.2 Determination of Primary Design Parameters

As a step towards designing the discrete planar varactor diode array chip for the 55/110 GHz frequency doubler, the primary design parameters needed to be determined. Specifically, the desired doping levels for the buffer layer and epitaxial layer (N_{buffer} and N_d respectively) were to be ascertained. Also, the optimum buffer layer thickness, t_{buffer}, and the optimum epitaxial layer thickness, t_{epi}, were to be selected. The process of selecting these parameters is addressed in the following paragraphs.

There are several material systems with varying buffer and epitaxial layer thicknesses and doping levels that are in use in the industry. As noted earlier, buffer layer doping levels of the order of 10^{18} cm^{-3} and epitaxial layer doping levels in the range from 10^{16} cm^{-3} to 10^{17} cm^{-3} are most suitable for millimeter and submillimeter-wave work. Figure-2.9 shows the skin depth in

the buffer layer as a function of frequency for doping levels of $1 \times 10^{18}\ cm^{-3}$, $2 \times 10^{18}\ cm^{-3}$ and $5.5 \times 10^{18}\ cm^{-3}$. These values were computed using Equation-2.18.

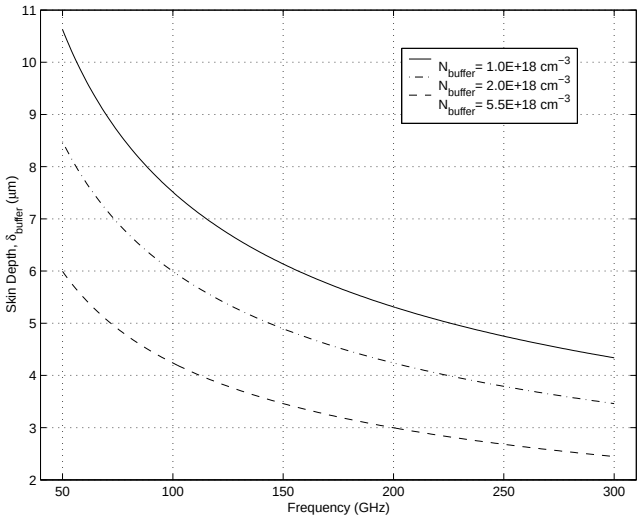

Figure 2.9: Plot of skin depth in the buffer layer vs. frequency for three doping levels.

Since the larger skin depths occur at lower frequencies, the choice of the buffer layer thickness and doping level was based on the lowest frequency of operation (i.e. the doubler input frequency of 55 GHz). In order to minimize the series parasitic resistance, the buffer layer doping was chosen to be as high as possible. $N_{buffer} = 5.5 \times 10^{18}\ cm^{-3}$ was selected because it represents the upper limit of doping level in commercially available material systems. The thickness of the buffer layer, t_{buffer}, had to be chosen to be more than the skin depth which is about 6 μm. Buffer layer thicknesses greater than 8 μm, being difficult to grow, are hard to find. Therefore $t_{buffer} = 8\ \mu m$ was selected. This satisfied the condition that the maximum skin depth be smaller than the buffer layer thickness.

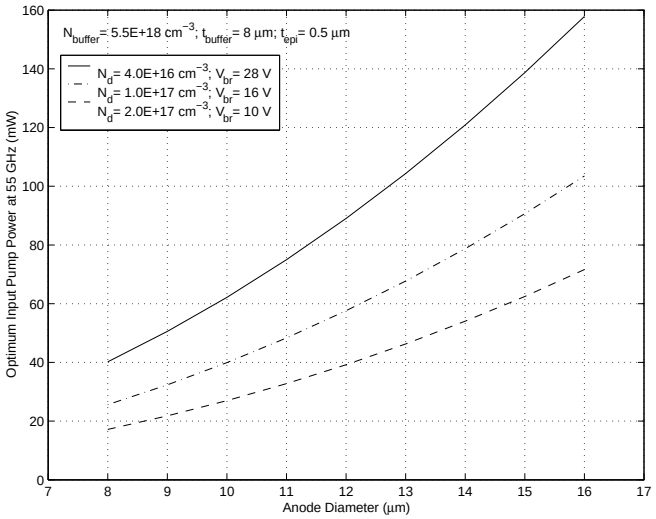

Figure 2.10: Input power (per diode) to obtain maximum conversion efficiency, for different anode sizes and epitaxial layer doping level.

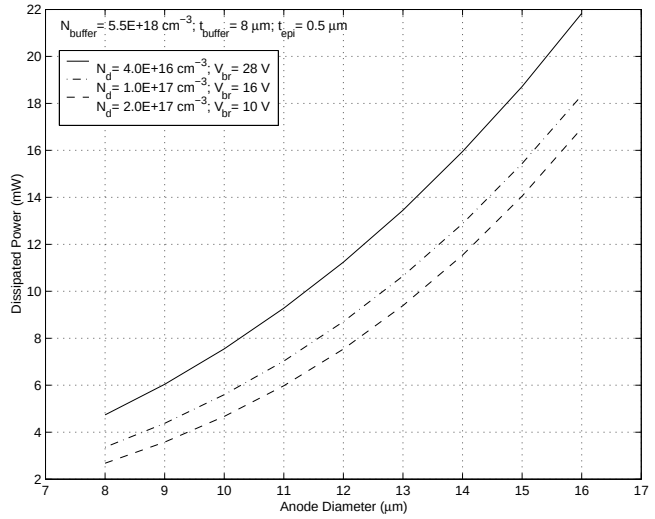

Figure 2.11: Power dissipated (per diode) under conditions of optimum operation for different anode sizes and epitaxial layer doping level.

The choice of the epitaxial layer thickness and doping level was not quite as straightforward. The decision was dependent on the input pump power handling capability desired, and interconnected with the choice of the size of

the junction as well as the number of diodes in the configuration. Figure-2.10 shows the input power levels required to maximize the conversion efficiency for a range of anode sizes and for three commonly available epitaxial layer doping levels. These results were obtained from one-tone harmonic balance simulations, performed using Hewlett Packard's Microwave and RF Design System (MDS) [145], for a single diode presented with optimum input and output embedding impedances and pumped at an input frequency of 55 GHz. The diode model that was used included only the parasitic series resistance (as calculated from Equation-2.13), and the zero bias junction capacitance (as calculated from Equation-2.12). The reverse breakdown voltages used in these calculations were obtained from Figure-2.6. Figure-2.11 shows the corresponding dissipated power levels.

From these data it is evident that lower level of epitaxial layer doping results in a higher input power handling capability. However, the power dissipated in the diode is also correspondingly higher. Tentatively, a value of $N_d = 1.0 \times 10^{17}\ cm^{-3}$ was chosen as a compromise between high input power handling capability and low dissipated power level.

Figure-2.12 shows the variation of depletion region width in the epitaxial layer at breakdown as a function of epitaxial layer doping, N_d. The depletion region widths were computed from Equation-2.9 using the reverse breakdown voltages given in Figure-2.6.

The epitaxial layer thickness was required to be as small as possible but larger than the maximum width of the depletion layer in order to avoid punch-through. Inspection of the depletion region widths at breakdown in Figure-2.12, led to the choice of $t_{epi} = 0.5\ \mu m$.

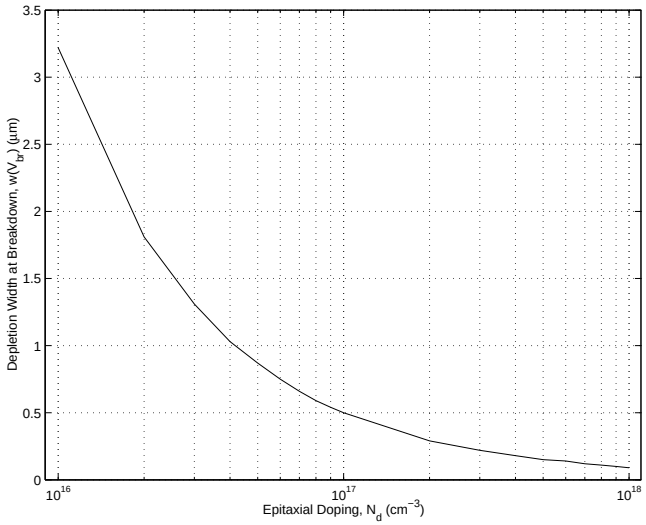

Figure 2.12: Variation of the width of the depleted region in the epitaxial layer at before breakdown as a function of epitaxial doping level.

These choices of N_d and t_{epi} were further justified during the process of selecting the number of diodes and choosing the anode size to be used. This is discussed next as a final step towards completing the specification of the diode array for the 55/110 GHz frequency doubler.

2.4.3 Design of the Planar Discrete Diode Array

Having obtained the specifications for the material system, the next step in the design of the diode array was the choice of anode size and determining the number of diodes needed. Figure-2.13, which shows the optimum input power levels as a function of a range of anode sizes for the chosen material system, was used for this purpose. The difference between the data in this plot and the one presented in Figure-2.10 is that the actual measured reverse breakdown voltage of 12 V was used in computing Figure-2.13 as opposed

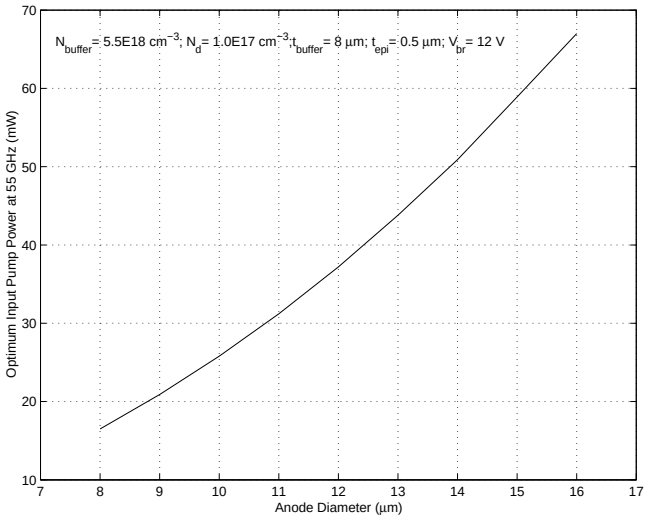

Figure 2.13: Input power (per diode) to obtain maximum conversion efficiency for a range of anode sizes for the chosen material system.

to the theoretical value of 16 V used earlier. This lowering of breakdown voltage was attributed to edge effects and inter-facial defects. The embedding impedances required for the best conversion efficiency are shown in Figure-2.14.

As before, larger anode sizes imply higher optimum input power levels. The Gunn-diode based oscillator intended to drive the frequency doubler had an output power of around 210 mW. The balanced configuration of Figure-2.2 required that the diode array consist of an even number of diodes. Inspection of the optimum input power levels presented in Figure-2.13 reveals that a balanced array comprised of six diodes with anode sizes in the range of $12 - 14\ \mu m$ could easily meet the requirement, while requiring reasonable input and output embedding impedances. The UVA SB13T1 balanced planar diode array, shown in Figure-2.15, met these specifications and was chosen for this work. It consisted of two branches each having three diodes in series.

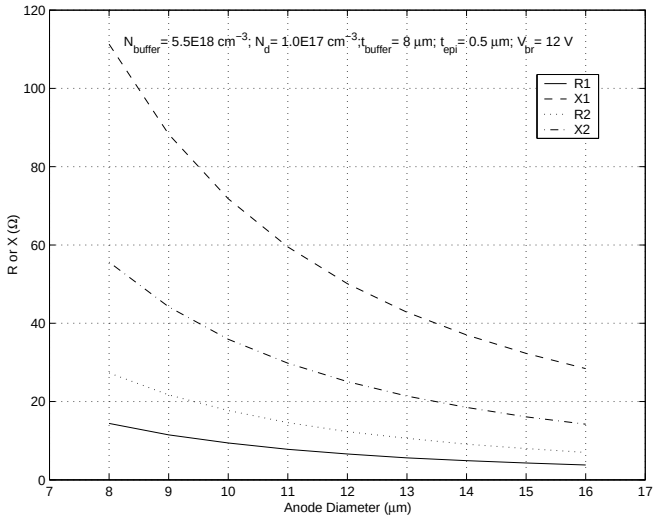

Figure 2.14: Optimum embedding impedances as a function of anode size.

The two branches were connected in an anti-serial manner, to realize the balanced configuration of Figure-2.2. This chip had an epitaxial layer doping (N_d) of $1.0 \times 10^{17}\ cm^{-3}$, an epitaxial layer thickness (t_{epi}) of 0.5 μm, a buffer layer doping (N_{buffer}) of $5.5 \times 10^{18}\ cm^{-3}$, and a buffer layer thickness (t_{buffer}) of 8 μm. The semi-insulating GaAs substrate was about 50 μm thick. The overall chip dimensions were 800 $\mu m \times 90\ \mu m \times 50\ \mu m$. For the 13 μm anode size the calculated parasitic series resistance, R_s, was 0.7 Ω and the zero bias junction capacitance, C_{j0}, was 138 fF. Its reverse breakdown voltage was measured to be 12 V per anode.

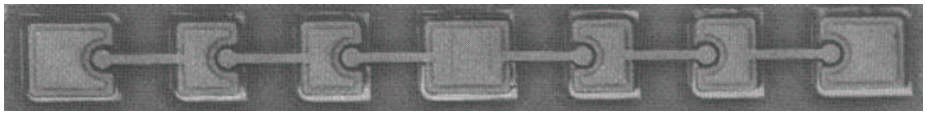

Figure 2.15: A Scanning Electron Micrograph of the UVA SB13T1 discrete planar Schottky varactor array used for the 55/110 GHz frequency doubler design.

2.5 Linear Embedding Circuit Design

In this section the process used to design the linear embedding circuit for the 55/110 GHz frequency doubler is described. The embedding circuit was implemented as a planar quartz circuit (to which the discrete planar diode array was attached) seated in a metal mount. All the modeling and simulations were carried out using Hewlett Packard's High Frequency Structure Simulator (HP-HFSS) [146] and MDS.

The anti-series arrangement of diodes on the UVA SB13T1 diode array (which results in the harmonic separation of input and output signals) allowed the design process to be divided into two smaller and mutually independent design tasks. The first part required the design of a suitable waveguide based input circuit (to allow the input pump power in a balanced mode), and the second part required the design of a planar quartz based output circuit (to couple the second harmonic power out of the diode array in an unbalanced TEM mode).

The following subsection provides a brief overview of the HP-HFSS software and the techniques employed to accurately model the UVA SB13T1 diode array using the software. The design of the input and output embedding circuits is presented in subsequent subsections.

2.5.1 HP High Frequency Structure Simulator (HP-HFSS)

The software uses the finite element analysis technique which divides the complete three-dimensional problem space into thousands of smaller regions

and represents the field in each sub-region with separate equations. In the simulator, the geometric model is automatically divided into a large number of tetrahedra, or four sided pyramids. The collection of tetrahedra is referred to as the finite element mesh.

The value of the vector field quantities (E- and H- fields) at points inside each tetrahedron is interpolated from the vertices of the tetrahedron. At each vertex, the simulator stores the components of the field that are tangential to the three edges of the tetrahedron. In addition, the system also stores the component of the vector field at the midpoint of selected edges that is tangential to a face and normal to the edge. The field inside each tetrahedron is interpolated from these nodal values. In this manner, Maxwell's equations are transformed into matrix equations and solved numerically. The output of the solver is in the form of a N-port scattering matrix.

A fine mesh (small tetrahedra) results in an accurate solution whereas a solution generated using a coarser mesh (larger tetrahedra) is less accurate. However, defining a fine mesh increases the number of tetrahedra required to represent a given three dimensional model and requires more memory to contain the representation matrix. To optimize the use of available computer memory, HP-HFSS initially uses a coarse mesh and then adaptively refines the mesh till the desired solution accuracy is achieved. The solution time depends on the amount of available computer memory, the speed of the computer, the size of the the structure with respect to the wavelength at the solution frequency, as well as the relation of the size of the smallest feature to the largest feature on the model. Thus to keep the solution time short, the size of the structure should be kept as small as possible.

In the case of a frequency doubler, where the output frequency is twice of the input frequency, the size of the structure with respect to the smallest wavelength could be quite large. Besides, the aspect ratio (i.e. the ratio of the largest to the smallest feature size) could result in a long solution time. To overcome this problem, the complete frequency doubler model was subdivided into smaller structures (that logically represented a certain function) and solved individually. The N-port solution scattering matrices were then recombined and optimized using MDS, to complete the design process.

Ports

In HP-HFSS, ports are special two dimensional boundaries which can be used to excite and absorb the electro-magnetic fields in a three dimensional model. HP-HFSS computes the solution S-matrices at the defined port boundaries. If more than one mode is found to be propagating at a boundary, HP-HFSS assigns a separate "virtual port" corresponding to each mode and proceeds to compute a multi-port solution, provided those modes have been selected by the user. Otherwise an error is flagged, and the modes are considered shorted at the port for the purpose of computing the solution. For the frequency doubler design, all the ports used on the subdivided structures were ensured to be single moded so that there was one to one correspondence between the physical ports on the model and the ports in the resulting solution matrix.

Probes

HP-HFSS requires that all the port definitions be at the interface of the three dimensional model structure with the external environment. This posed a problem – to calculate the impedance in the proximity of the Schottky junction, there was a need to be able to define ports at the location of the metal-epitaxial layer interface which was not exposed to the external environment. This limitation was overcome by treating the buffer layer, the circuit metalization, and the bond wires as perfect conductors and subtracting those structures from the overall three dimensional model. This operation caused the interior of these structures to be turned into an "external environment" while retaining the perfect conductor boundary condition at their surface. This enabled the placement of "coaxial probes" (within this newly created external environment) to estimate the impedance in the proximity of each of the six Schottky junctions. This geometry is shown in Figure-2.16. The actual S-parameters at the location of the Schottky junction could then be computed by de-embedding the length of the coaxial probes from the solution matrix.

Porting of HP-HFSS data to MDS

As mentioned earlier, the output of the HP-HFSS simulator is in the form of generalized scattering matrix which describes the scattered waves present at each of the ports, under the assumption that the ports are connected to transmission lines having identical geometries as the ports themselves. By default, the scattering matrix is normalized with respect to 50 Ω. However in order to allow the solutions for the various substructures to be combined

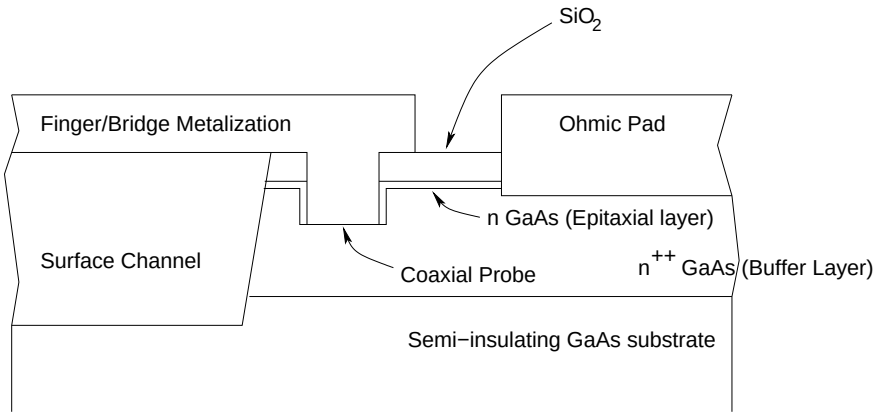

Figure 2.16: The coaxial probe geometry employed to calculate the impedance at the location of the Schottky junctions.

meaningfully in MDS, there was a need to re-normalize the solutions with respect to the port impedances. HP-HFSS has a choice of three port characteristic impedance definitions for this purpose – Z_{pi}, Z_{pv}, and Z_{vi}. These are defined as follows

$$Z_{pi} = \frac{P}{\mid I \mid^2} \tag{2.21}$$

$$Z_{pv} = \frac{VV^*}{P} \tag{2.22}$$

$$Z_{vi} = \sqrt{Z_{pi} Z_{pv}} \tag{2.23}$$

where P, $\mid I \mid$ and V can be computed from

$$P = \oint_S \vec{E} \times \vec{H^*}.\vec{ds} \tag{2.24}$$

$$\mid I \mid = \frac{1}{2} \oint_l \mid \vec{H}.\vec{dl} \mid \tag{2.25}$$

$$V = \int_l \vec{E}.\vec{dl} \tag{2.26}$$

Z_{pi} relates the impedance to the power crossing a cross section and the line integral of the current around the cross section. Unlike Z_{pv} (and therefore Z_{vi} by definition), it does not depend on the choice of a user defined impedance line to compute a path-integral and is always calculated by HP-HFSS by default. It was therefore used to re-normalize the computed scattering matrix prior to exporting data to a Touchstone- or Citifile- format output file for use in MDS.

2.5.2 Design of the Input Section

The operation of the frequency doubler was described in Section-2.3. Figure-2.17 illustrates the design of the input embedding circuit of the frequency doubler. The coaxial probes, described earlier, were used to attach ports at each of the six Schottky junction locations in the diode array.

The input was chosen to be a WR-19 (U-Band) waveguide which propagates the 55 GHz input towards the diode array as a balanced TE_{10} dominant mode. The dimensions of the rectangular cross section of the standard waveguide, being fixed, did not need to be optimized. The reduced height section of waveguide placed between the full height input waveguide and the location of the diodes served as an impedance transformer to transform the impedance of the input waveguide to a suitable impedance required to be presented to the diode array. The length of this reduced height section (marked d_2 in Figure-2.17) was used as a design variable and optimized. The full height input waveguide could support several balanced modes at the output fre-

quency (such as TM_{01}). The reduced height section was designed to be cut off for those modes and caused them to evanesce and not couple any second harmonic power towards the input port. The height of this section was chosen based on the above criteria, and set to one-quarter of full height after some experimentation. The distance of the input back-short (marked d_1 in Figure-2.17) on the other side of the diode array, where the input reduced height waveguide ended, was another variable that was optimized to obtain a good input match. The effect of the small rectangular opening in the input back-short, corresponding to the output channel, was insignificant since the channel was too small to support the input TE_{10} mode. The thickness and size of the GaAs dielectric being set by the size of the diode array, was not subject to optimization. Similarly, the thickness of the planar quartz circuit was empirically chosen to be 5 mil and not optimized.

Optimum diode embedding impedance at input frequency, as given in Figure-2.14, was attached to each of the diode ports (ports 2 thru 7) and the lengths d_1 and d_2 were optimized in MDS to get a good (15 - 20 dB) return loss at port-1.

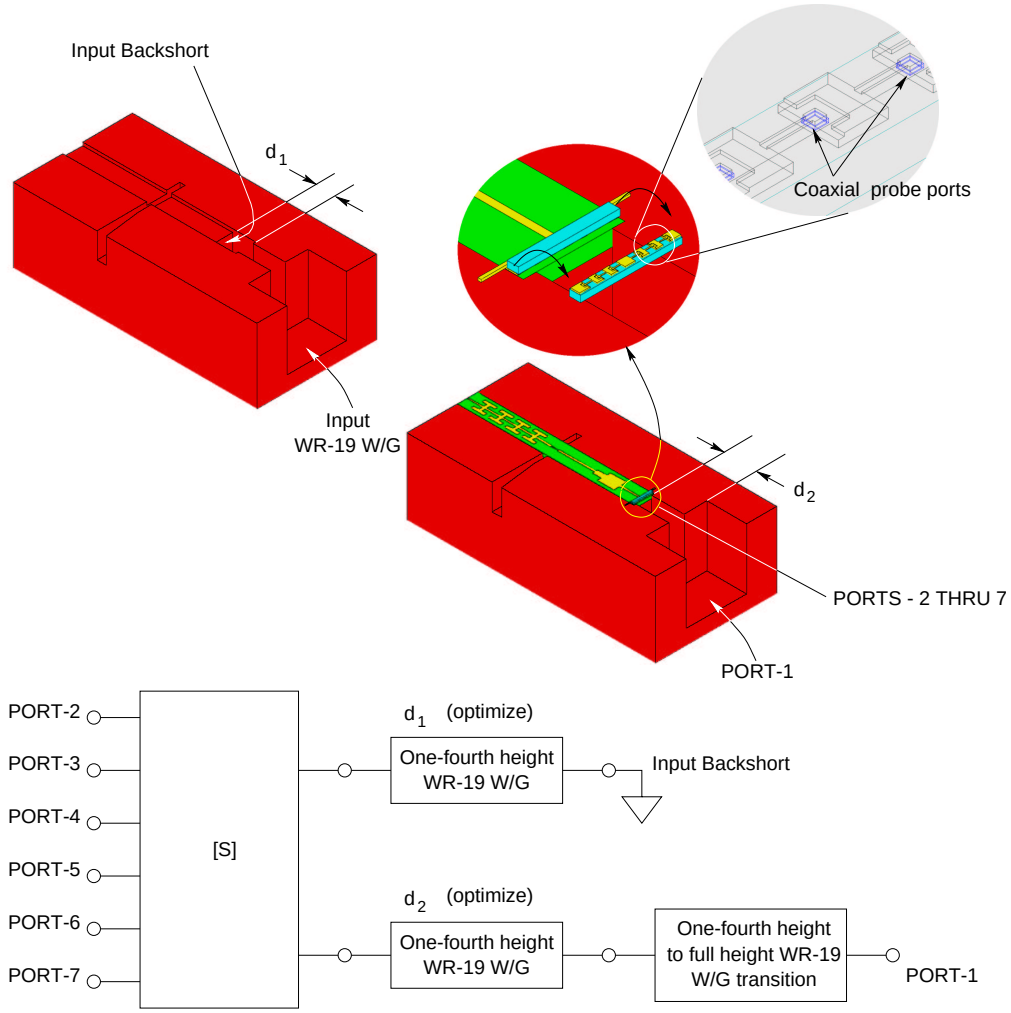

Figure 2.17: Design of the input embedding circuit for the 55/110 GHz frequency doubler. Only bottom half of the mount that seats the quartz circuit is shown, with and without the quartz circuit in place. The location of various ports as well as the dimensions that were optimized are illustrated. The equivalent circuit model schematic (based on the S-parameter files generated by HP-HFSS) used in MDS to optimize the lengths d_1 and d_2 in the input circuit is shown at the bottom.

2.5.3 Design of the Output Section

The output circuit consisted of a quasi-coaxial section in the reduced height input waveguide followed by two microstrip impedance transforming sections that matched the diode array to a 50 Ω microstrip. The 50 Ω microstrip coupled into the reduced height output waveguide and was also attached to the DC bias filter. The design of the output coupler and the DC bias filter is addressed later. Figure-2.18 illustrates the design of the impedance matching part of the output embedding circuit. As done while designing the input embedding circuit, coaxial probes were used to attach ports at each of the six Schottky junction locations in the diode array.

Optimum diode embedding impedance at output frequency, as given in Figure-2.14 was attached to each of the diode ports (ports 2 thru 7) and the lengths d_3 and d_4 optimized in MDS to get a good (15 - 20 dB) return loss at port-1.

The effect of balanced modes (such as TE_{10}, TE_{20} etc.) in the reduced height input waveguide was ignored since those modes were unlikely to be excited, given the symmetric nature of the diode geometry.

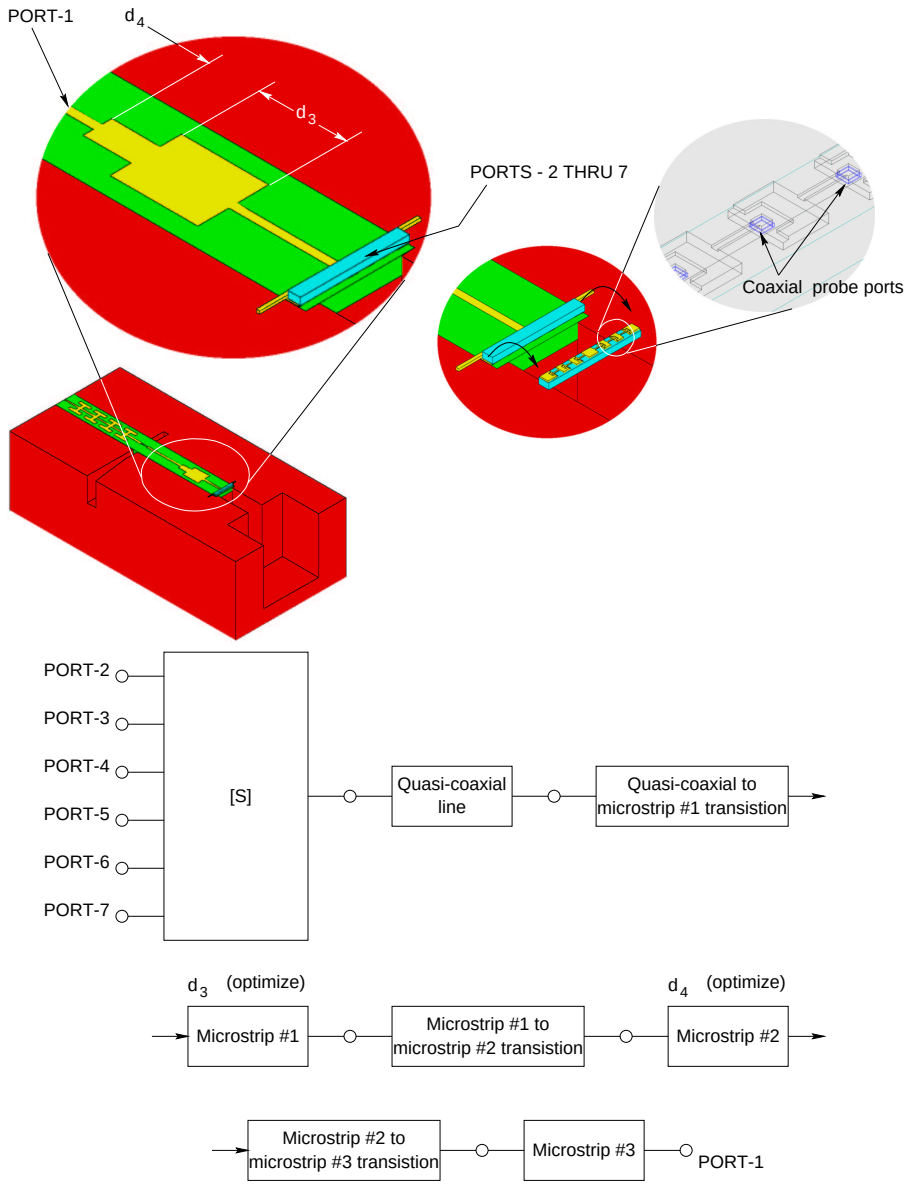

Figure 2.18: Design optimization of the impedance matching sections of the output embedding circuit for the 55/110 GHz frequency doubler. Only bottom half of the mount that seats the quartz circuit is shown. The location of various ports as well as the dimensions that were optimized are illustrated. The equivalent circuit model schematic (based on the S-parameter files generated by HP-HFSS) used in MDS to optimize the lengths d_3 and d_4 in the output circuit is shown at the bottom.

2.5.4 Design of the DC Bias Filter

The DC bias filter consisted of four "hammer head" sections in cascade and served to provide adequate RF isolation for the DC bias port. Since the DC bias line was an extension of the microstrip metalization on the output quartz circuit, the filter was designed and optimized for a "band stop" function at the output frequency of the frequency doubler. Figure-2.19 illustrates the various dimensions that were optimized in HP-HFSS. Figure-2.20 has a plot of S_{21} for the resulting design.

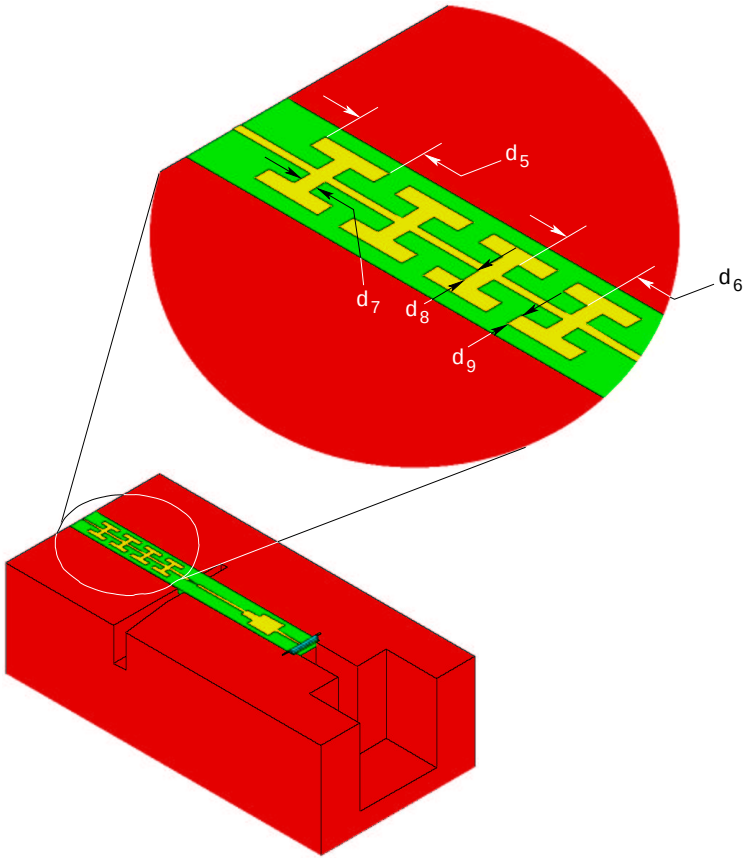

Figure 2.19: Design of the bias filter. Only bottom half of the mount that seats the quartz circuit is shown. All the dimensions that were optimized are marked.

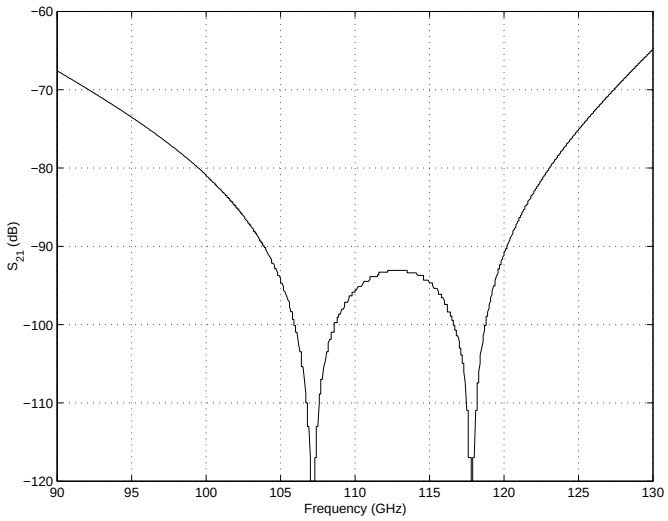

Figure 2.20: Plot of S_{21} for the DC bias filter (simulated).

2.5.5 Design of the Output Waveguide Taper

For reasons described later, the waveguide in the microstrip to waveguide coupler was a one-fifth height section of WR-8 (F-Band) waveguide. However, the frequency doubler output flange was to be a standard WR-8 waveguide section. A linear taper was employed to transition from one-fifth height to full height waveguide. The linear taper was optimized to yield a good input match (return loss of about 20 dB) for the smallest possible length of the taper section. This involved performing a series of simulations in HP-HFSS with different lengths for the taper section and selecting the shortest taper length meeting the above criteria. Figure-2.21 shows S_{11} for the chosen taper length.

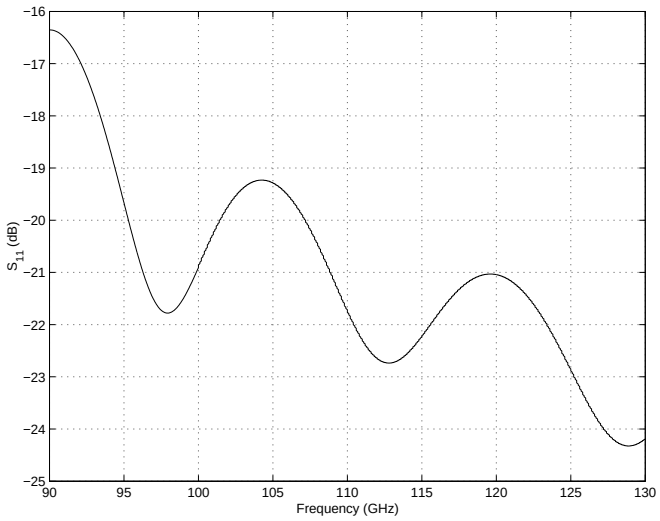

Figure 2.21: Plot of S_{11} for the WR-8 one-fifth to full height waveguide linear taper (simulated).

2.5.6 Design of the Output Microstrip to Waveguide Coupler

The microstrip to waveguide coupler was designed at the very end, so as to be able to account for the effects of the DC bias filter and the output waveguide linear taper on the coupling arrangement. Power was coupled into a one-fifth height section of a WR-8 (F-Band) waveguide, which was chosen to maximize the coupling bandwidth. Figure-2.22 illustrates the geometric parameters that were optimized in HP-HFSS and MDS to perform this design. Figure-2.23 and 2.24 respectively show the resulting S_{11} and S_{21} for the completed design.

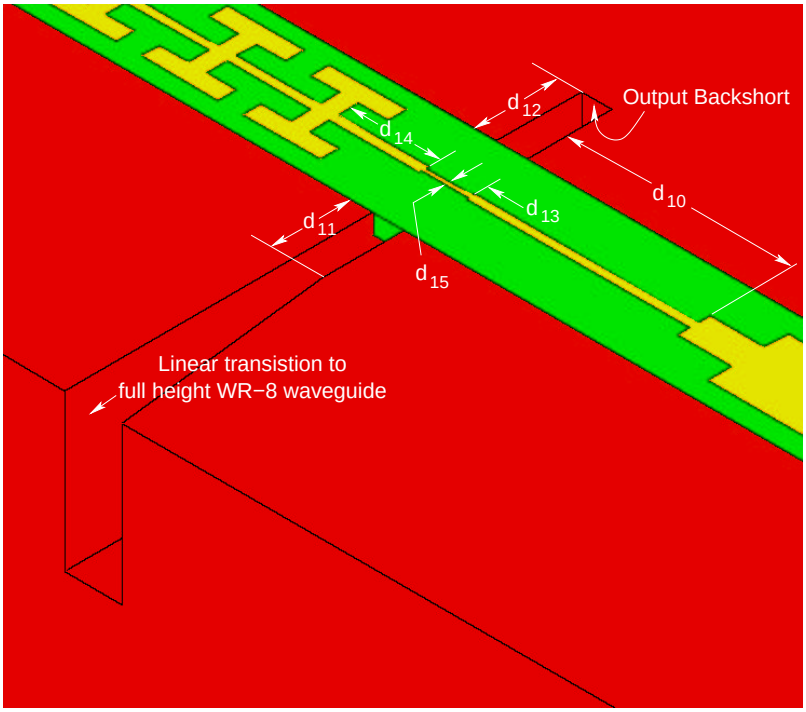

Figure 2.22: Design of the output cross-guide coupler for the 55/110 GHz frequency doubler. Only bottom half of the mount that seats the quartz circuit is shown. The dimensions that were optimized to achieve a good coupling efficiency are marked.

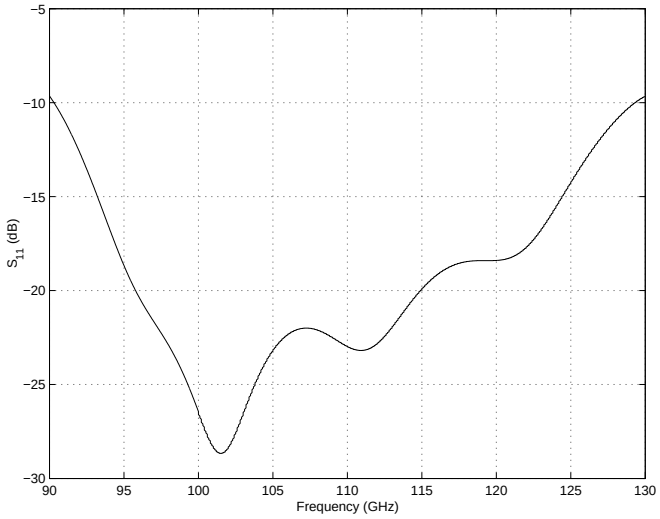

Figure 2.23: Plot of S_{11} for the complete output coupling arrangement, including the microstrip to one-fifth height waveguide probe, DC-bias filter and the one-fifth height to full height taper (simulated).

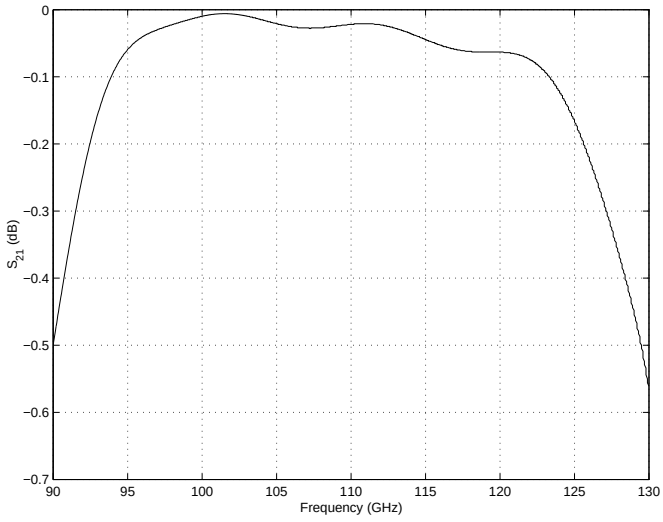

Figure 2.24: Plot of S_{21} for the complete output coupling arrangement, including the microstrip to one-fifth height waveguide probe, DC-bias filter and the one-fifth height to full height taper (simulated).

2.6 Fabrication and Assembly

The planar quartz circuit, to which the diode array was to be attached was fabricated on a 5 mil thick fused-quartz substrate using a photolithographic process. The mask was fabricated on a 3 inch $\times$ 3 inch $\times$ 0.060 inch chromium soda-lime substrate and was right reading, chromium down, dark field type. The mechanical drawings of the mask used in the process are provided in Appendix-B. As shown in these drawings, three variations of the planar circuit were included on the same mask. One variation was optimized for an output frequency that was 5 GHz above the nominal output frequency of 110 GHz, while the other was optimized for an output of 5 GHz below the nominal output frequency. The procedure for the photolithographic fabrication of the circuits is provided in Appendix-C.

The metallic housing for the frequency doubler circuit was machined as a split block. To allow fabrication using standard milling techniques, each half was fabricated in three pieces and subsequently assembled. The mechanical drawings of the split block pieces and their assembly are provided in Appendix-D.

A description of the procedure to attach the UVA SB13T1 discrete planar diode array to the planar quartz circuit and their subsequent housing into the metal block is provided in Appendix-E.

The evaluation of the completed frequency doubler is described in the following section.

2.7 Evaluation

The evaluation of the 55/110 GHz frequency doubler was carried out by driving it with a frequency tunable klystron oscillator and measuring the generated output power using an appropriate power sensor and meter. The details of the arrangement are illustrated in Figure-2.25 and explained below.

The isolator following the klystron oscillator source served to prevent any reflected power emanating from the rest of the experimental setup from coupling back into the klystron and affecting its performance. The precision attenuator was used as a power leveling device and was set appropriately to equalize the input power to the frequency doubler over the range of input frequencies. The directional coupler and the spectrum analyzer served two functions. They were used to measure and set the frequency of the klystron oscillator as well as to estimate the input reflection coefficient of the frequency doubler. The calibration short placed on port "A" of the waveguide switch was used to set the "reference" level for making the reflection coefficient measurement. The HP V8486A power meter sensor attached to port "B" of the waveguide switch was used to measure and set the input power level to the frequency doubler, which was itself connected to port "C" of the waveguide switch. The output of the frequency doubler, appearing at section identified as "D" in the figure, was measured using an Anritsu F-Band power sensor.

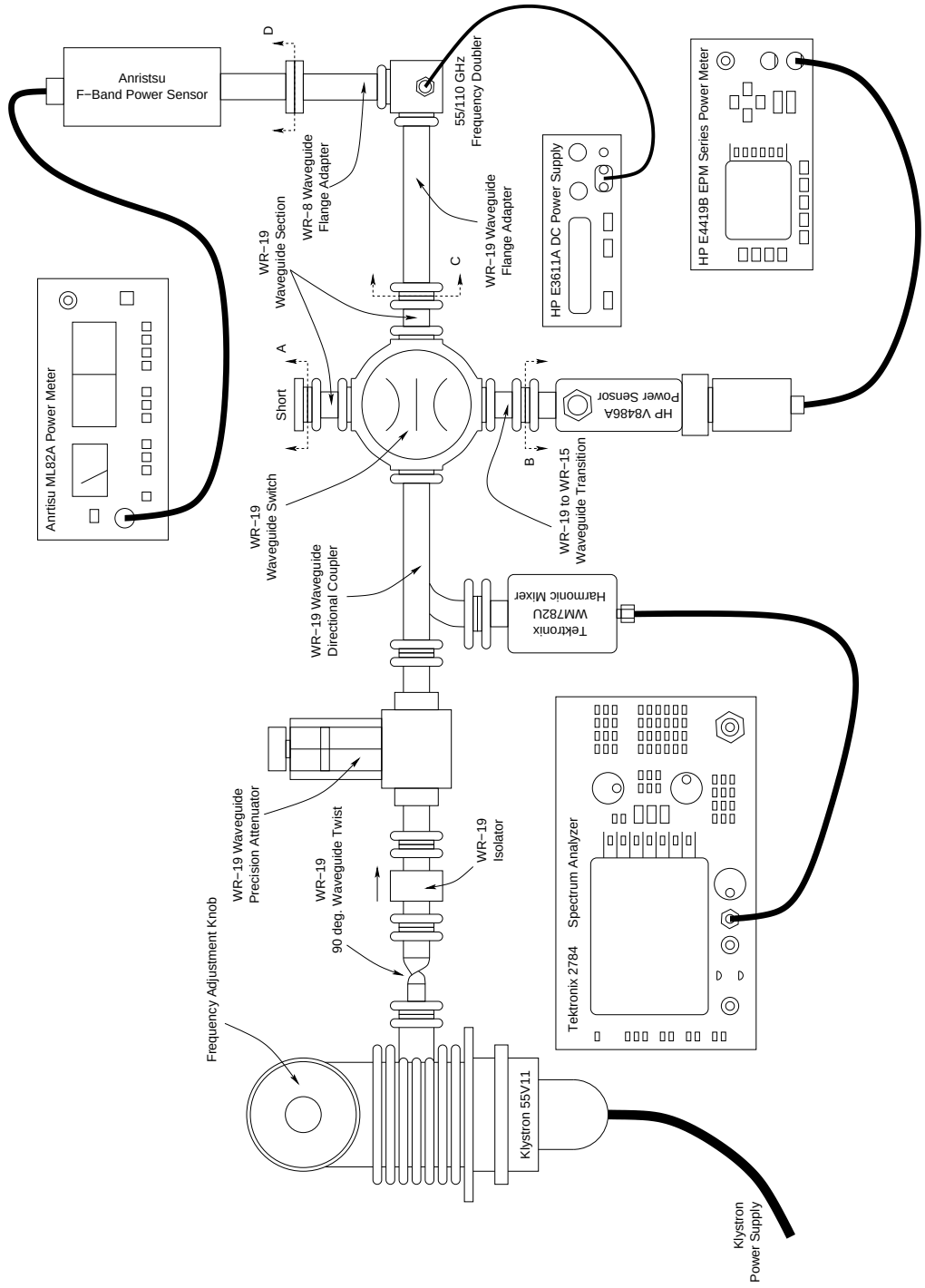

Figure 2.25: Experimental setup for evaluation of the 55/110 GHz frequency doubler.

The input of the frequency doubler was referenced to port "C" while its output was referenced to "D". The input WR-19 flange adapter and the output WR-8 flange adapter were considered integral to the frequency doubler for the purpose of measuring the input and output power levels and computing its flange to flange efficiency. The frequency doubler was biased using a DC power supply and the bias current and voltage levels were monitored.

Prior to commencing each measurement, the precision attenuator was set to maximum attenuation and the waveguide switch was set to connect port "B" to the klystron source. The frequency of the klystron oscillator was then set by observing the oscillation frequency on the spectrum analyzer. The attenuation setting on the precision attenuator was lowered to raise the signal level on the spectrum analyzer, if needed, taking care not to exceed the power rating of the HP V8486A power sensor. The reading on the HP E4419B power meter and the attenuator setting were recorded. The bias voltage to the frequency doubler was set to -18 V and the waveguide switch was set to connect the frequency doubler input (port "C") to the klystron source. The precision attenuator was adjusted to set the desired input drive level (based on the power level readings recorded earlier) to the frequency doubler. The bias was then adjusted to maximize the output power detected by the Anritsu F-Band power sensor connected at "D" and measured by the Anritsu ML82A power meter. The measured output power as well as the corresponding bias voltage were recorded. Finally the reflected signal level, as measured by the spectrum analyzer, was recorded and compared with the level appearing on the spectrum analyzer with the waveguide switch turned to place the reference short (at port "A") at the directional coupler output. This resulted in an estimate of the input return loss of the frequency doubler.

For output frequencies below and up to 110 GHz, the output power measurements of the Anritsu ML82A power meter (with the F-Band power sensor) were cross checked with the measurements made by HP E4419B EPM series power meter. The HP W8486A W-Band power sensor (not shown in the figure) was connected to section "D" instead of the Anritsu F-Band power sensor for this purpose. The use of a WR-10 waveguide power sensor to perform measurements on a WR-8 waveguide was not expected to impair the measurements since the capacitive and inductive discontinuities due to a change in the waveguide height and width (respectively) at the junction of the two waveguides tend to anti-resonate and cancel each other out [150].

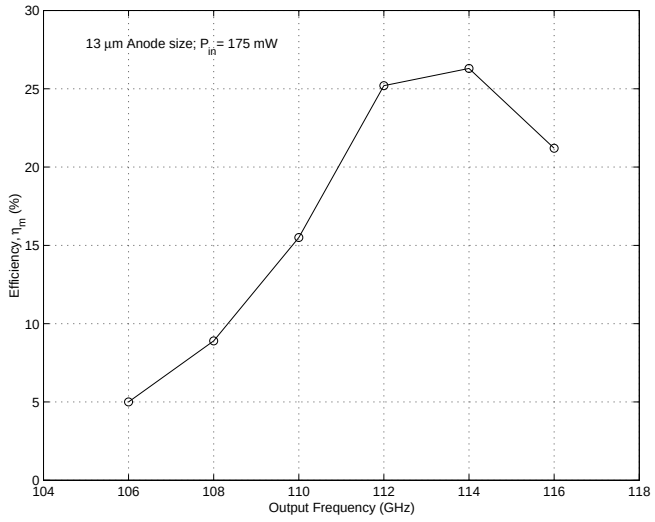

Figure 2.26: Measured conversion efficiency of the 55/110 GHz frequency doubler using a diode array with 13 μm diameter anodes.

Figure-2.26 shows the measured conversion efficiency of the 55/110 GHz frequency doubler constructed using a UVA SB13T1 diode array with 13 μm diameter (nominal) anode size, with an input power of 175 mW. This input power level was chosen to maximize the measurement frequency range, given

the limited output power bandwidth of the klystron oscillator source. The best efficiency was measured at an output frequency of 114 GHz, higher than the nominal design frequency of 110 GHz. This was consistent with measured value of the zero bias junction capacitance for the diodes in the array which was lesser than the designed/calculated value. The measured "per anode" zero bias junction capacitance was about 120 fF, lower than its calculated value of 138 fF used in the harmonic balance simulations performed to design the frequency doubler. This deficiency of junction capacitance was also reflected in the lower than expected bias voltages required to maximize the conversion efficiency. For a measured breakdown voltage of 12 V per anode the correct operating bias voltage should have been about 18 V, half of the breakdown voltage for three diodes in series, so as to allow for equal voltage swings on either side of the operating point. The measured values of bias voltages needed to maximize the conversion efficiency were significantly lower, as shown in Figure-2.27.

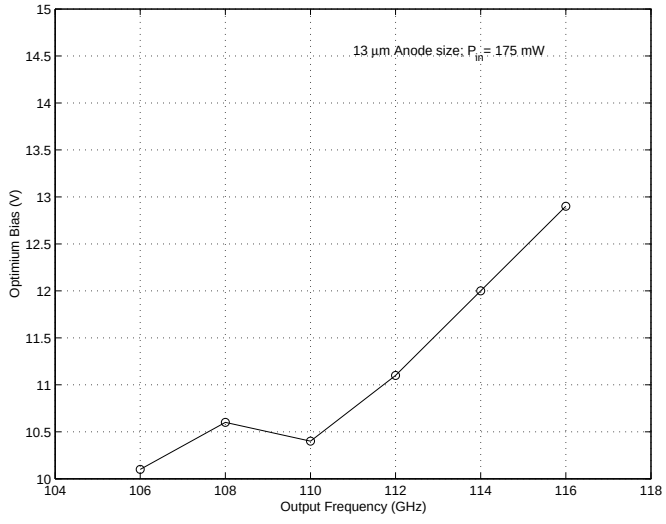

Figure 2.27: Plot of the measured optimum bias voltage versus output frequency.

Measurements of the output power and conversion efficiency were also made as a function of input pump power level at an output frequency of 114 GHz (corresponding to the highest conversion efficiency in Figure-2.26). Figure-2.28 shows the results of these measurements. No saturation in the output power level was noticeable for an input power up to 210 mW, consistent with the predicted power handling capacity of 260 mW for the six-diode array based on the data presented in Figure-2.13 earlier.

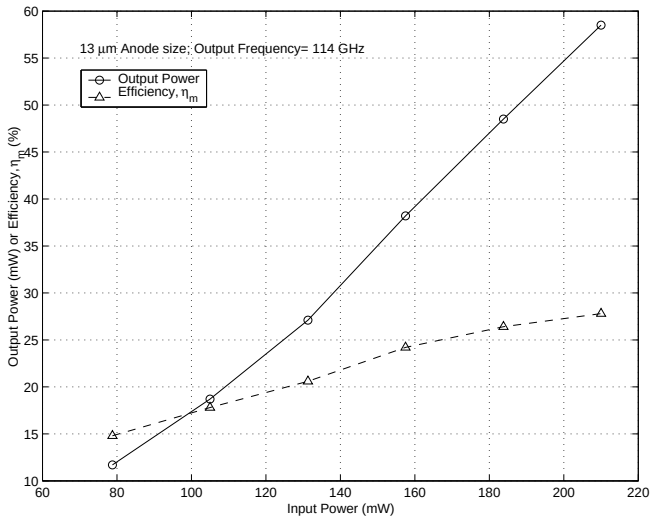

Figure 2.28: Measured output power and efficiency versus input pump power for an output frequency of 114 GHz.

Finally, the 55/110 frequency doubler block was rebuilt using a diode array with 14 μm diameter junctions. Figure-2.29 shows the measured output power versus frequency for this unit, illustrating the fact that the increased junction capacitance (due to the larger anode size) had the desired effect of moving the frequency of peak efficiency downward to 110 GHz.

The results presented in this section are analyzed together with those from the evaluation of the 110/220 GHz frequency doubler in Section-2.9. The 110/220 GHz frequency doubler is described next in the following section.

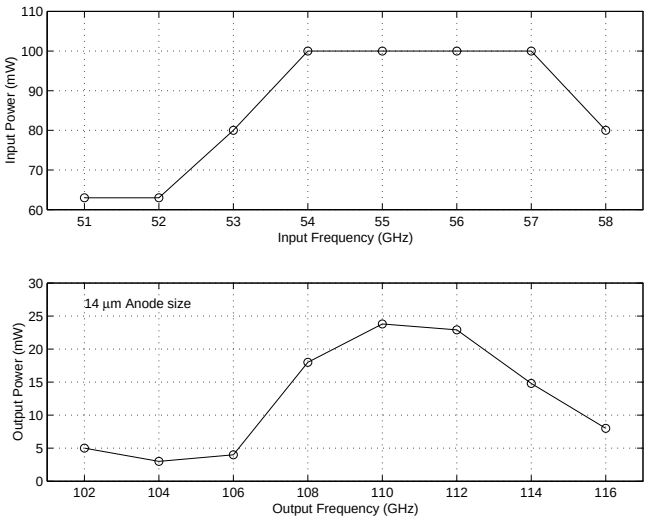

Figure 2.29: Plot of the measured output power versus frequency for the 55/110 GHz frequency doubler using a diode array with 14 μm diameter anodes.

2.8 The 110/220 GHz Frequency Doubler

This section presents the details of design, fabrication, and evaluation of a 110/220 GHz frequency doubler. This frequency doubler was based on a circuit configuration very similar to the one used for the 55/110 GHz frequency doubler. The techniques used to design the discrete planar diode array as well as its embedding network were very similar to those used for the 55/110 GHz frequency doubler as well. Consequently only a brief summary of the design procedure, together with pertinent design data, is presented here.

2.8.1 Planar Schottky Varactor Design

As before, the doping level of the buffer layer (N_{buffer}) was chosen to be $5.5 \times 10^{18}\ cm^{-3}$ to minimize the parasitic resistance. The buffer thickness (t_{buffer}) was selected to be 5 μm, so as to be greater than the skin depth for the chosen doping level at input frequency, using the plots in Figure-2.9.

Figure-2.30 presents the optimum input power levels required to maximize the conversion efficiency for a range of anode sizes and three different epitaxial layer doping levels. Figure-2.31 shows the corresponding dissipated power levels. As before, these data was the result of one-tone harmonic balance simulations.

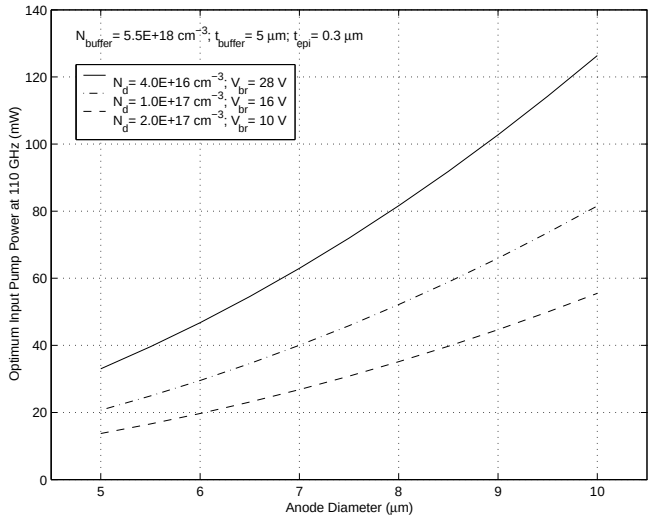

Figure 2.30: Input power (per diode) to obtain maximum conversion efficiency, for different anode sizes and epitaxial layer doping level.

The 110/220 GHz frequency doubler was intended for operation with an input drive power of about 100 mW. Inspection of data presented in Figure-2.30 and 2.31 reveals that a balanced four diode configuration with an anode diameter of 7 μm could meet this requirement with minimum dissipated power per anode, for an epitaxial doping level of 2.0×10^{17} cm^{-3}. The epitaxial layer thickness was selected to be 0.3 μm based on the width of the depletion layer at reverse breakdown from the data presented in Figure-2.6.

Figure-2.32 shows the optimum input power levels (per anode) for this choice of parameters. The measured reverse breakdown voltage of 9 V was

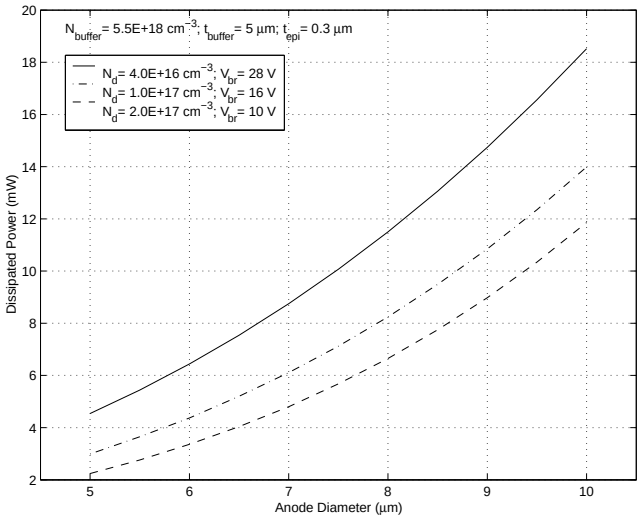

Figure 2.31: Power dissipated (per diode) under conditions of optimum operation for different anode sizes and epitaxial layer doping level.

used in performing these harmonic balance calculations instead of the theoretical value of 10 V used earlier.

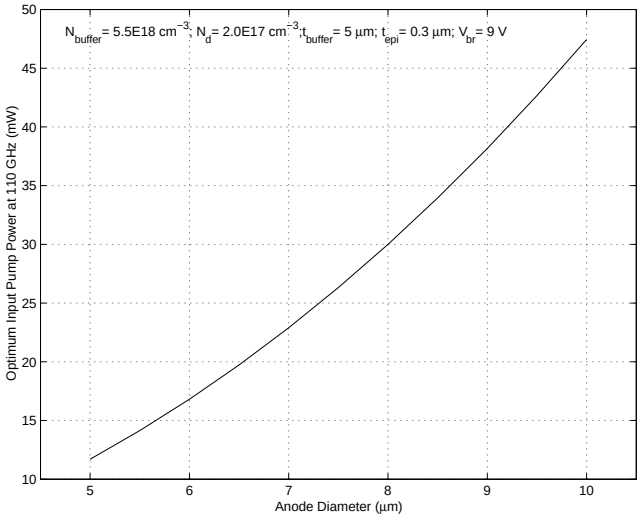

Figure 2.32: Input power (per diode) to obtain maximum conversion efficiency for a range of anode sizes for the chosen material system.

The optimum embedding impedances required are presented in Figure-2.33. Three variations of the discrete planar diode array (anode sizes of 6 μm, 7 μm, and 8 μm) were fabricated. For the nominal 7 μm anode size the calculated parasitic series resistance, R_s, was 0.8 Ω and the zero bias junction capacitance, C_{j0}, was 56 fF. Its reverse breakdown voltage was measured to be 9 V per anode. The overall chip dimensions were 400 $\mu m \times 60$ $\mu m \times 70$ μm.

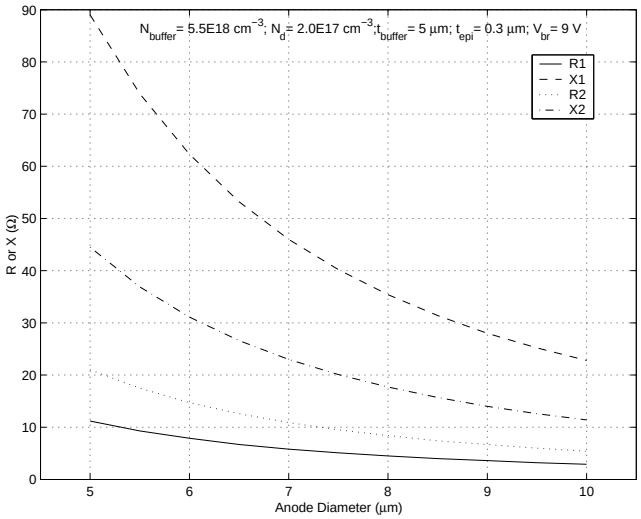

Figure 2.33: Optimum embedding impedances as a function of anode size.

Figure 2.34: A Photograph of the UVA SB7T7 discrete planar Schottky varactor array used for the 110/220 GHz frequency doubler design.

2.8.2 Linear Embedding Circuit Design

As was the case with the 55/110 GHz frequency doubler, the linear embedding circuit consisted of a planar quartz circuit placed in a waveguide block. The input was a WR-8 (F-Band) waveguide, while the output was a WR-4 waveguide. The reduced height section of the input waveguide in the input embedding network was a one fifth height section of standard WR-8 waveguide. Similarly, the output microstrip to waveguide transition was designed for a one fifth height section of standard WR-4 waveguide.

The strategy employed to design the embedding circuit was same as the one employed earlier for the design of the 55/110 GHz frequency doubler. The input and output impedance matching networks were designed to match the optimal diode embedding impedances of Figure-2.33 placed at the "diode ports".

Figure-2.35 shows S_{21} for the "hammer head" DC bias filter. The input return loss of the one fifth height to full WR-4 waveguide transition is presented in Figure-2.36, while Figure-2.37 and 2.38 show the S_{11} and S_{21}, respectively, of the complete output coupling arrangement including the bias filter, the output back-short, and the output waveguide taper.

2.8.3 Fabrication and Assembly

The planar quartz circuit to which the diode array was to be attached, was fabricated on a 2 mil thick fused-quartz substrate using a photolithographic process. The mask for this purpose was fabricated as a part of the 55/110 GHz frequency doubler mask set. The mechanical drawings of the mask are provided in Appendix-B. As indicated on these drawings, seven variations of

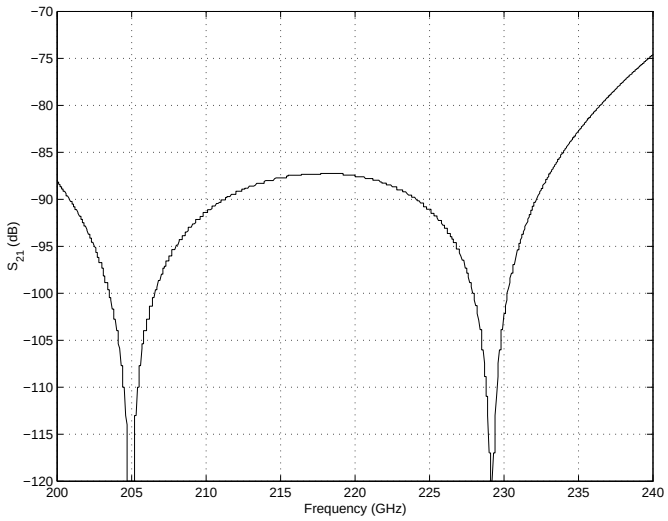

Figure 2.35: Plot of S_{21} for the DC bias filter (simulated).

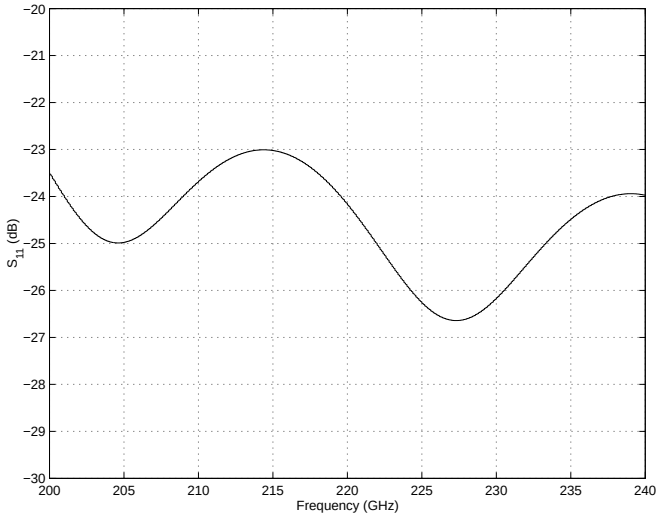

Figure 2.36: Plot of S_{11} for the WR-4 one-fifth to full height waveguide linear taper (simulated).

the planar circuit were included on the same mask. Three of the variations were optimized for an output frequencies that was above the nominal output frequency of 220 GHz while the remaining three were optimized for an out-

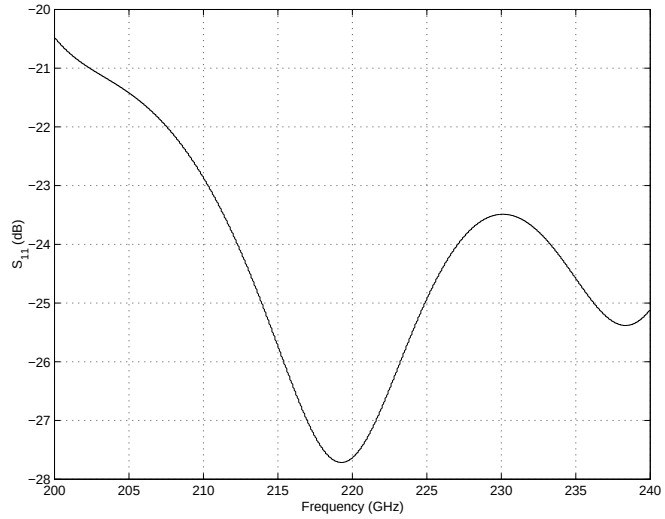

Figure 2.37: Plot of S_{11} for the complete output coupling arrangement, including the microstrip to one-fifth height waveguide probe, DC-bias filter and the one-fifth height to full height taper (simulated).

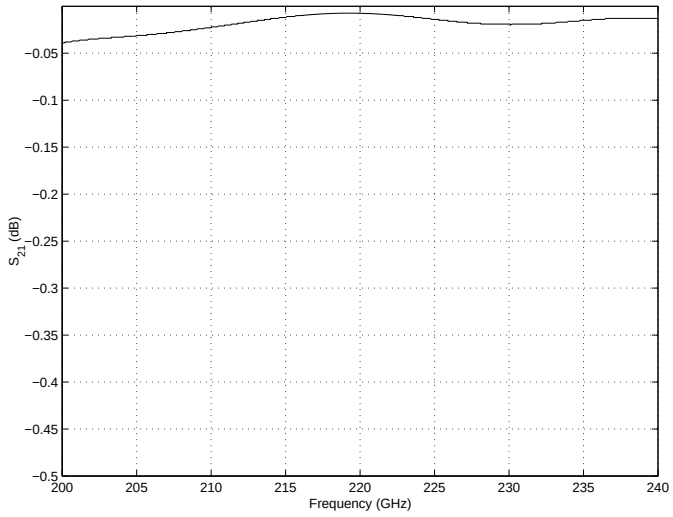

Figure 2.38: Plot of S_{21} for the complete output coupling arrangement, including the microstrip to one-fifth height waveguide probe, DC-bias filter and the one-fifth height to full height taper (simulated).

put frequency below the nominal output frequency. The procedure for the photolithographic fabrication of the circuits is provided in Appendix-C.

The metallic housing for the doubler circuit was fabricated as a split block by electro-forming. The mechanical drawings of the mandrel around which copper was electro-deposited as well as the details of the final split pieces and their assembly are provided in Appendix-D.

A description of the procedure to attach the discrete planar diode array to the planar quartz circuit and their subsequent housing into the metal block is provided in Appendix-E.

2.8.4 Evaluation

The evaluation of the 110/220 GHz frequency doubler was carried out by driving it with the output of the 55/110 GHz frequency doubler and measuring the generated output power using an appropriate power meter and sensor. As before, the 55/110 GHz frequency doubler was driven by a frequency tunable klystron oscillator. The details of the arrangement are illustrated in Figure-2.39 and explained below.

The isolator following the klystron oscillator source served to prevent any reflected power emanating from the rest of the experimental setup from coupling back into the klystron and effecting its performance.

The precision attenuator was used at its high attenuation setting to effectively "switch off" power input to the 55/110 GHz frequency doubler while making adjustments between successive measurements. It was set to zero attenuation while making the measurements so as to provide maximum drive power to the 55/110 GHz frequency doubler and hence to the 110/220 GHz

frequency doubler under test. The directional coupler and the spectrum analyzer were used to measure and set the frequency of the klystron oscillator. The input to the 110/220 GHz frequency doubler was measured by attaching the F-Band Anritsu power sensor (not shown in the figure) at section marked "A" and recording the power read by the Anritsu ML82A power meter. The output of the 110/220 GHz frequency doubler was measured using a G-Band Anritsu power sensor at the section marked "B" and recording the power read by the Anritsu ML82A power meter.

The input of the frequency doubler was referenced to the flange at "A" while its output was referenced to that at "B". The input WR-8 flange adapter and the output WR-4 flange adapter were considered integral to the frequency doubler for the purpose of measuring the input and output power levels and computing its flange to flange efficiency. The frequency doubler was biased using a precision bias power supply and the bias current and voltage levels were monitored.

Prior to each measurement, the precision attenuator was set to maximum attenuation and the 110/220 GHz frequency doubler was detached at section "A" and replaced by the F-Band Anritsu power sensor (not shown in the figure). The attenuation of the precision attenuator was then reduced somewhat, to allow setting the desired input frequency by observing the oscillation frequency on the spectrum analyzer and adjusting the klystron controls. Subsequently, the attenuation was reduced to zero and the 55/110 GHz bias voltage was adjusted to maximize its output drive power as detected by the F-Band Anritsu sensor connected at "A" and measured by the Anritsu ML82A power meter. This drive level was recorded and the precision

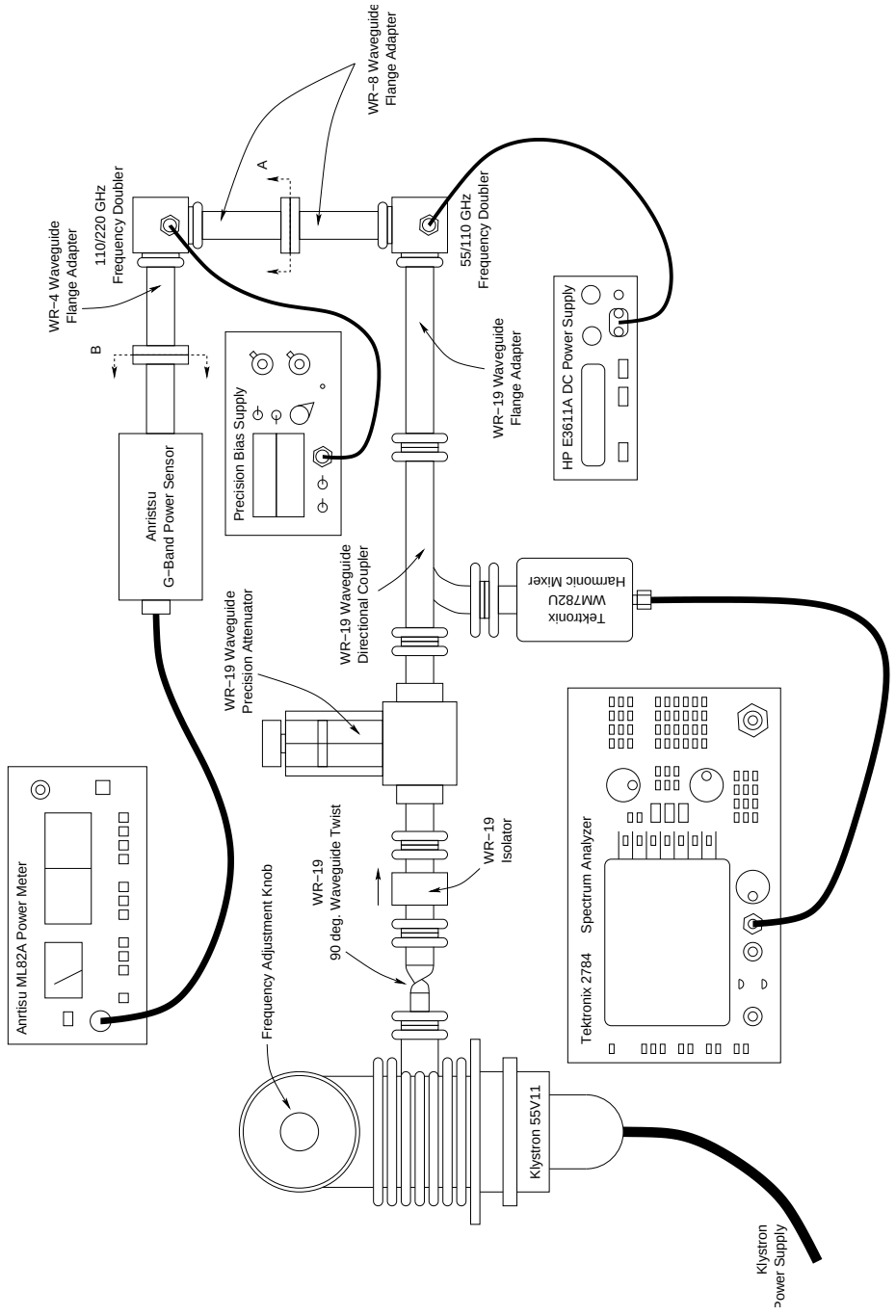

Figure 2.39: Experimental setup for evaluation of the 110/220 GHz frequency doubler.

attenuator returned to its maximum attenuation state. The Anritsu F-Band power sensor was then detached and the 110/220 GHz frequency doubler input was reconnected at "A". A waveguide switch was avoided here in order to minimize the losses and provide maximum possible drive to the frequency doubler under evaluation. The attenuator was returned to its zero attenuation setting and the output of the the 110/220 GHz frequency doubler, as detected by the Anritsu G-Band power sensor and measured by the Anritsu ML82A power meter, was recorded. The precision bias supply was adjusted to maximize the doubling efficiency.

The measured performance of the 110/220 GHz frequency doubler, constructed using a diode array with 8 μm diameter anodes, is presented in Figure-2.40. The input power levels are also shown. The 8 μm anode size was chosen over the nominal 7 μm anode size called for by the design because the measured zero bias junction capacitance of the diodes with 7 μm diameter anodes was much less than the expected 56 fF per anode. The zero bias junction capacitance of the diodes with 8 μm diameter anodes was measured to be 53 fF. (This was less than the calculated value of 73 fF for this anode size, perhaps symptomatic of a possible under-cutting of the epitaxial layer.)

Measurements were made both in the varactor mode (with the diodes reverse biased as usual) of operation and in the varistor mode (with the diodes forward biased) of operation. For output frequencies below 224 GHz, the output power in the varistor mode of operation exceeded that in the varactor mode of operation and vice versa.

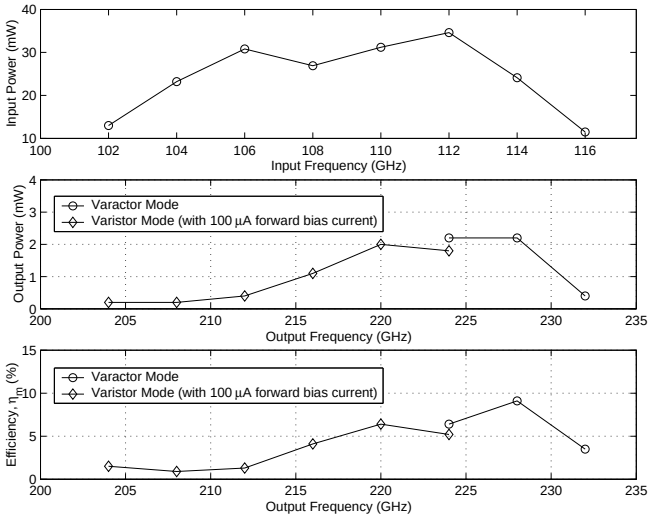

Figure 2.40: Measured performance of the 110/220 GHz frequency doubler, built using a diode array having anodes with 8 μm diameter.

2.9 Discussion of Results

Though both the 55/110 GHz and the 110/220 GHz frequency doublers were successfully built based on the hybrid approach and subsequently evaluated, several factors were uncovered during the design and fabrication process that had an adverse effect on their performance. These factors, discussed below, tended to be more significant for the 110/220 GHz frequency doubler indicating that the hybrid design approach was less suitable for high frequency multiplier work.

The input impedance matching depended solely on the machining accuracy of waveguide structures in the metal block. While it is relatively easy to maintain a high degree of accuracy for large structures, the same was not true for much smaller structures required for this work. For instance, in order to machine the housing for the 55/110 GHz frequency doubler by

conventional machining techniques, it was necessary to fabricate each half of the split block in three separate pieces. The assembly of these pieces, however precise, still left significant crevices along the mating surfaces which could have adversely effected the operational efficiency. Furthermore, conventional machining was not suitable at all for manufacturing the housing for the 110/220 GHz frequency doubler due to its even smaller size. This block had to be manufactured by electro-depositing copper on a carefully machined aluminum mandrel. This approach had its own drawbacks. Precise machining of an aluminum mandrel was a challenging task, as was the the task of machining precise mating surfaces between the two halves made of electro-deposited copper. In the block used for the evaluation of the 110/220 GHz frequency doubler, the mating of the two pieces in several critical regions around the diode array was quite questionable. This could have been one of the contributing factors towards the low conversion efficiency measured for this frequency doubler. The monolithic approach offers the possibility of realizing all the impedance matching structures as planar circuits instead of precisely machined waveguide structures and should therefore be more advantageous for high frequency multiplier work.

Flip mounting the diode array on planar quartz circuits (as described in Appendix-E) was a tedious process and introduced uncertainties that could not be easily modeled at the design stage. For instance, the amount of solder used to attach the diode array to the quartz circuit introduced parasitics that were difficult to model or predict. Furthermore, the effect of these parasitics was likely to have been more severe on the 110/220 GHz frequency doubler design where the percentage variation introduced would be larger due to

the smaller size of the circuit structures. A monolithic approach could do away with such "low level" assembly tasks, eliminating one possible source of uncertainty, making it more suitable for high frequency designs.

The 110/220 GHz frequency doubler design called for thinner bond wires than the ones used in the 55/110 GHz frequency doubler. However both the designs had to be optimized with 0.7 mil diameter bond wires, which was the minimum available size. Such restrictions place a serious limitation on the designer's ability to optimize higher frequency designs. Furthermore, it was observed that the actual bond-wire length used for grounding of the diode array could only be ensured to be approximately equal to its designed value. Any departure in the bond-wire length was significant because it was in the RF path. Since inductive reactance scales with frequency, the effect of such a departure in bond-wire length would have been more pronounced on the 110/220 GHz frequency doubler. As shall be seen later, the monolithic approach offers alternate grounding techniques that could eliminate the need for critical length bond-wires making it a better approach for engineering high frequency designs.

Figure-2.41 shows the best realized efficiencies for frequency doublers based on the hybrid approach, as a function of output frequency. It clearly illustrates the limitation of the applicability of this approach for high frequency multiplier designs.

2.10 Conclusion

The design of a 55/110 GHz frequency doubler and a 110/220 GHz frequency doubler based on the hybrid design approach and their implementation and

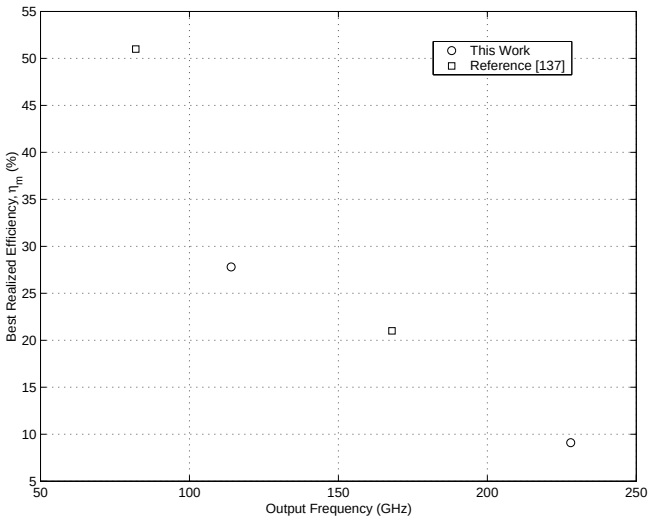

Figure 2.41: Plot of the best reported and measured efficiencies of various frequency doublers built based on the hybrid approach.

evaluation was presented in this chapter. Based on the shortcomings of these designs, the limitations of this approach for high frequency multiplier work were identified and a case made for an investigation of the monolithic approach for the design of millimeter- and submillimieter-wave frequency multipliers.

Besides overcoming the various disadvantages of the hybrid approach as described in the previous section, the MMIC approach has some other benefits as well. With all of the circuit being realized as one single chip, this approach should yield designs that are much easier to assemble and do not require complicated assembly. This would have a positive impact on the repeatability and reliability of the designs, making them more suitable for large scale production. The MMIC approach should be inherently better suited to balanced designs requiring good device symmetries as well as those requiring compact and low loss idler circuits.

The following chapter explores this design approach further. It describes the work done to develop the circuit elements needed to make it practical, and subsequently sets the stage for the design of an integrated 80/240 GHz frequency tripler.

Chapter 3

Monolithic Technology

The advantages of planar MMIC type frequency multipliers were amply borne out by the discussion toward the end of Chapter-2. The investigation presented in this chapter focuses on the selection of a suitable substrate and material system as well as the development and evaluation of integrated circuit-element structures required for a successful execution of such a design.

3.1 Introduction

The design of a MMIC based frequency multiplier requires the choice of a suitable material system to allow for the design and fabrication of both the

linear and non-linear portions of the circuit alongside each other on a common substrate. Furthermore, the design of the planar embedding circuits is itself contingent upon the availability of suitable integrated circuit elements on the chosen substrate to synthesize the desired embedding network. Suspended microstrip, microstrip or coplanar waveguide could be employed as transmission lines to transport microwave power, while open- or short-circuited shunt stubs in the appropriate transmission line configuration could be used to fulfill the need for shunt tuning elements. Integrated inductor and capacitor elements would be required for series reactance tuning as well as for synthesis of other circuit functions. Furthermore, waveguide transitions would need to be designed to couple the pump signal from the waveguide into the circuit as well as to extract the desired harmonic power back into an appropriate waveguide. The following sections address each one of these requirements, and describe the selections made for the purpose of this research based on the evaluation of test structures.

3.2 Material System and Substrate

Due to its high electron mobility, GaAs based wafers represent the material system of choice for fabrication of diodes for millimeter- and submillimeter-wave multiplier applications. However GaAs material (which has a relative dielectric permittivity, ϵ_r, of approximately 13.1) causes dielectric loading of the channel in the waveguide block that houses the integrated circuit, causing higher order modes to propagate. Therefore, it needs to be modified to make it suitable for fabrication of monolithic multiplier circuits.

Techniques used to overcome the problem include backside wafer thinning [44], complete removal of the semi-insulating layer [35] (yielding substrate-less designs employing frames for mechanical support) as well as use of frame-less monolithic membrane diodes [37]. The backside wafer thinning technique results in a $20 - 40\ \mu m$ thick substrate which is generally acceptable for embedding circuit design, but makes the design of wide-band input and output waveguide couplers difficult due to the still significant dielectric loading effect. The framed substrate-less technology although very promising, requires specialized processing and is a relatively recent innovation. The same is also true for the monolithic membrane diode technology. Both of these technologies eliminate the adverse effects of the high dielectric constant substrate by removing it altogether, resulting in a fragile monolithic chip. However for applications beyond 300 GHz (and well into the THz region), the physical size of the complete chip tends to be small enough to permit its handling and assembly into a waveguide block. In the 100–300 GHz range however, the size of the chip could be rather large and cause mechanical problems. Besides, when used in designs calling for large input and dissipated power levels, the heat dissipation capabilities of such structures are also somewhat suspect.

The substrate employed in this research was of a composite nature, consisting of a GaAs membrane attached to a quartz carrier. The elimination of all of the semi-insulating GaAs substrate under the epitaxial and buffer layers alleviated the dielectric loading problems, while the quartz substrate provided mechanical strength as well as a thermal path for heat dissipation. The substrate fabrication was based on the Method of Adhesion by Spin-

on-dielectric Temperature Enhanced Reflow (MASTER), first developed at UVA in 2000 for integrated Schottky diode based mixers [151], and since modified [152] [153].

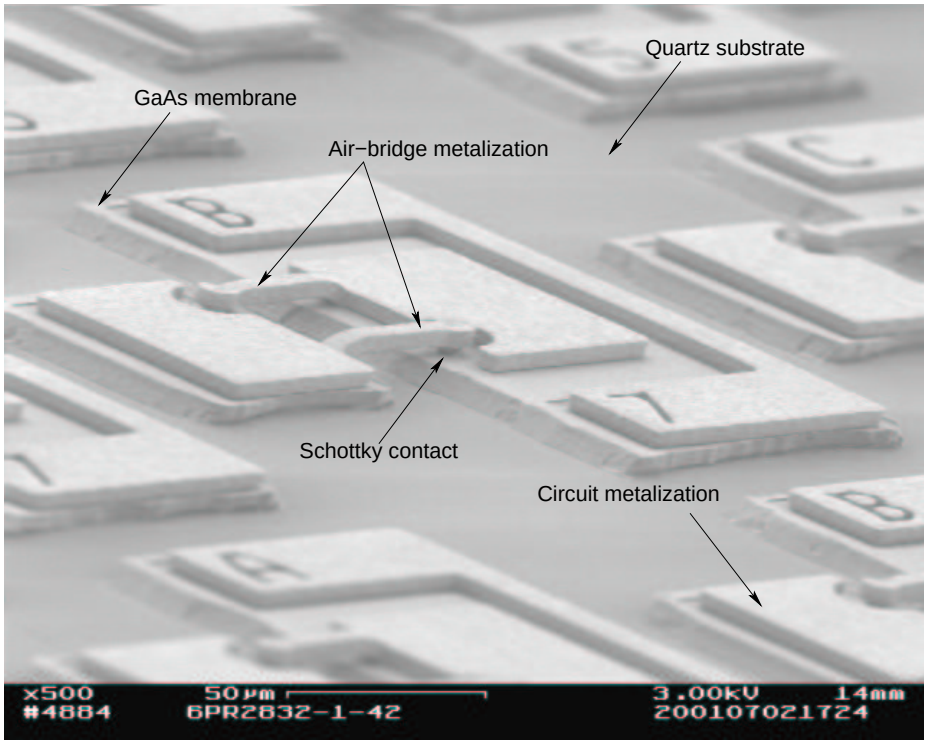

Figure 3.1: A Scanning Electron Micrograph of an undiced wafer fabricated based on the composite GaAs-membrane-on-quartz approach. Photograph courtesy Gerhard S. Schoenthal, University of Virginia, Semiconductor Development Laboratory.

Prior to any front side processing, the semi-insulating substrate of the GaAs wafer was removed via mechanical and chemical lapping. Using the UVA bonding process, this thinned GaAs epitaxial layer was then attached to a 10 mil quartz substrate using a spin on dielectric as an adhesion agent. This was followed by front side processing, to define the diode and circuit struc-

ture. The final step in the front side processing involved electro-deposition of gold to form anode and circuit metalization followed by a directional GaAs etch to achieve device separation on the wafer. Subsequently, the completed wafer was diced on the front side and chip separation achieved by lapping the backside down to a thickness of 2 mil. Figure-3.1 shows a photo of such a wafer prior to dicing, while Figure-3.2 is a photograph of the wafer after front side dicing but prior to chip separation by thinning of the wafer via backside mechanical lapping.

Figure 3.2: Photograph of the diced wafer prior to backside lapping to achieve chip separation. Photograph courtesy Gerhard S. Schoenthal, University of Virginia, Semiconductor Development Laboratory.

The relative dielectric permittivity of quartz is about 3.8 which was low enough to prevent the propagation of any higher order modes in the waveguide block channel. As was done in the case of hybrid-MIC frequency dou-

blers of Chapter-2 linear embedding circuits could be designed and optimized for the quartz substrate with the metalization corresponding to the circuit elements being performed at the same time and alongside the diode metalization, resulting in a monolithic frequency multiplier circuit.

3.3 Transmission Line

The coplanar waveguide, a suspended microstrip, and the microstrip structure were some of the choices available for the implementation of integrated transmission lines. The coplanar waveguide was not selected due to its requirement of a top-side ground plane, and the apparent difficulty of designing wide-band rectangular waveguide transitions for this transmission line structure. The suspended microstrip and microstrip transmission lines are similar structures, with the suspended microstrip exhibiting lower losses than the microstrip structure. Suspended microstrip however required additional machining of ledges in the channel to support the chip. For very shallow channels (like the 1 mil deep channels were used in the 80/240 GHz frequency tripler design), it could be difficult to machine long ledges to the desired degree of flatness. Consequently, microstrip type transmission lines, illustrated in Figure-3.3, were selected.

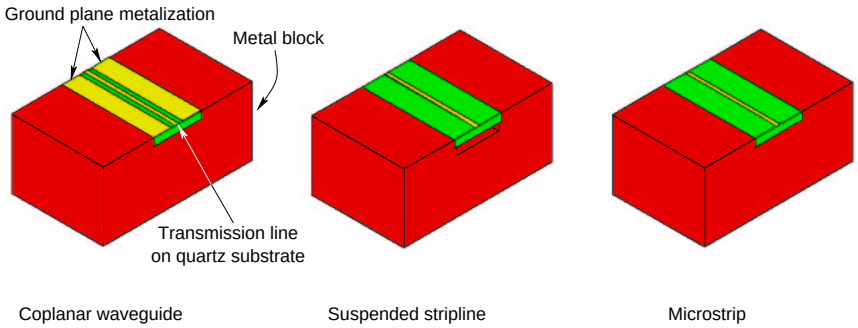

Figure 3.3: Planar transmission line structures.

3.4 Waveguide Transitions

In order to couple the microwave power to and from the planar circuit, rectangular waveguide to microstrip transitions similar to the one illustrated in Figure-3.4 were designed. This microstrip to WR-4 waveguide transition had a fixed back-short and consisted of a cantilevered probe arrangement in a reduced height section of the waveguide. The reduced height section of the waveguide was flared to the standard waveguide height that appeared at the flange. The length of this linear waveguide taper was the minimum length required to yield a return loss of at least 20 dB over the entire waveguide band. The position of the back-short was optimized to yield good coupling efficiency over the 170–260 GHz frequency range (WR-4 waveguide band). Figure-3.5 and 3.6 respectively show the calculated S_{11} and S_{21} for the 50 Ω microstrip to WR-4 rectangular waveguide transition of Figure-3.4. This particular design was employed as the output coupler in the 80/240 GHz frequency tripler block.

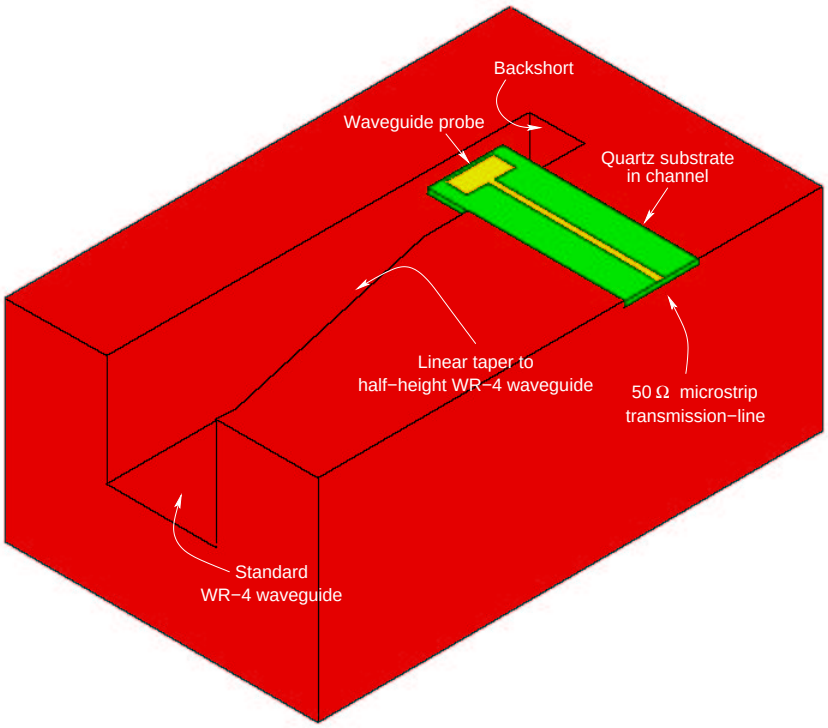

Figure 3.4: The microstrip to WR-4 waveguide transition. Figure shows a cut-away view of the arrangement. Only the bottom half of the block is illustrated, revealing the placement of the quartz circuit in the metal housing.

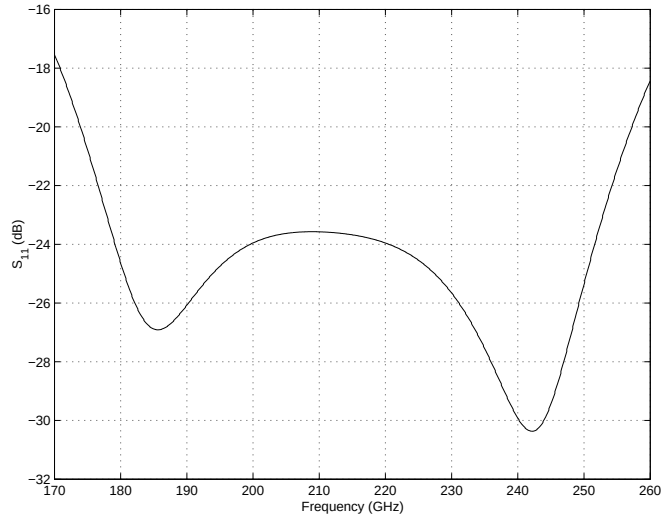

Figure 3.5: Plot of S_{11} for the microstrip to WR-4 waveguide transition of Figure-3.4.

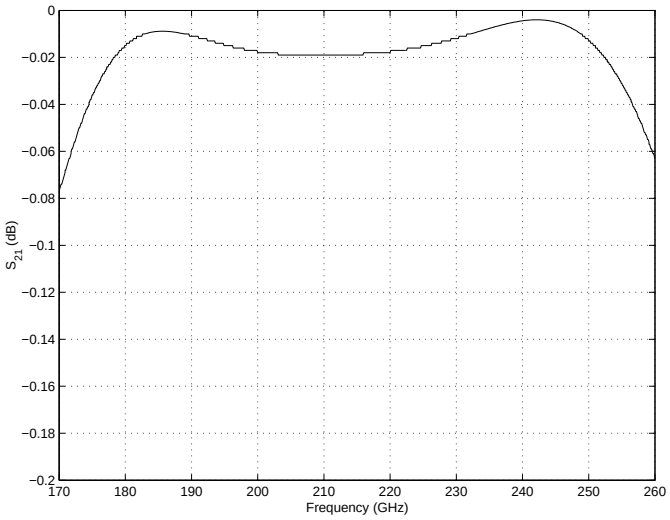

Figure 3.6: Plot of S_{21} for the microstrip to WR-4 waveguide transition of Figure-3.4.

3.5 Integrated Capacitors

Integrated capacitors are required as series reactance tuning elements as well as for RF coupling and DC bias arrangements on a monolithic design. They are generally realized as Metal-Insulator-Metal (MIM) structures on the wafer using sputter deposited SiO_2, Chemical Vapor Deposited (CVD) SiO_2, or SiN as the insulating material. The study presented in this section was performed to evaluate their usability in millimeter- and submillimeter-wave frequency multiplier applications, especially from the point of view of realizable specific capacitance and the associated loss. Since no published experimental data was to be found in this regard especially at higher frequencies, appropriate test structures had to be designed, fabricated, and evaluated. Measurements were performed in the W-Band (75–110 GHz frequency range) to obtain the relevant data. The loss was considered important because of its impact on the conversion efficiency of the frequency multiplier, more so due to the low available signal power, in general, at these frequencies.

3.5.1 Test Devices

MIM type test capacitor structures with the insulator material sandwiched between metal layers were fabricated using each of the three insulator materials listed above. The fabrication was done on a 2 mil thick fused-quartz substrate [154], that was subsequently mounted into a channel in a metallic test fixture. One terminal of the capacitor was grounded using EPO-TEK H20E silver epoxy [155] while the other plate was connected to a microstrip attached to a WR-10 waveguide probe as shown in Figure-3.7.

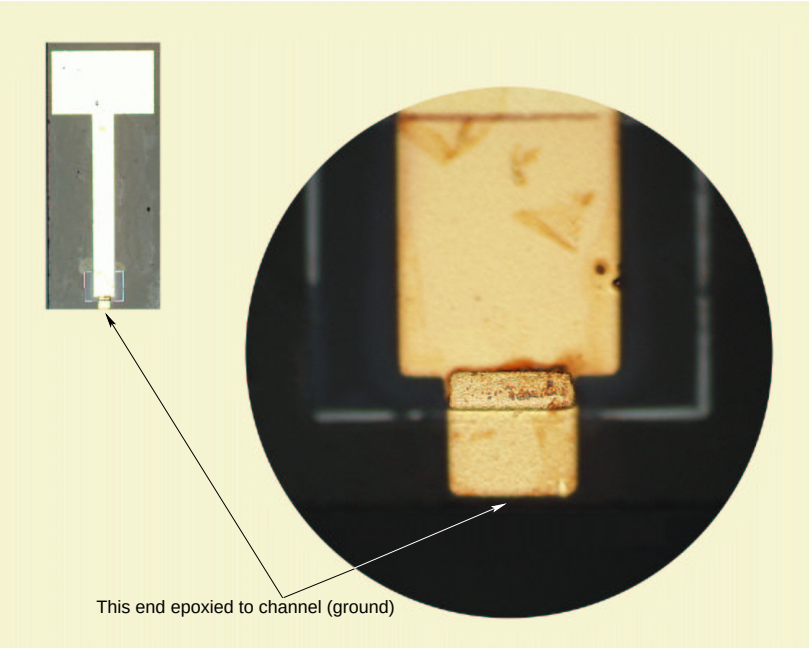

Figure 3.7: Photograph of 2 mil thick quartz circuit showing the test capacitor at one end of the microstrip transmission line. The waveguide probe is visible as a "flag" structure on the other end of the microstrip.

3.5.2 Experimental Setup

The test fixture consisted of a WR-10 waveguide section that was flared down to a quarter height waveguide section. The probe on the quartz circuit was positioned in this reduced height section (see Figure 3.8) and was designed for good coupling across entire W-Band. The reflection coefficient was measured at the waveguide flange using the HP8510C Network Analyzer, and the parameters for the capacitor under test computed numerically from these data. The computation procedure is described in the following section.

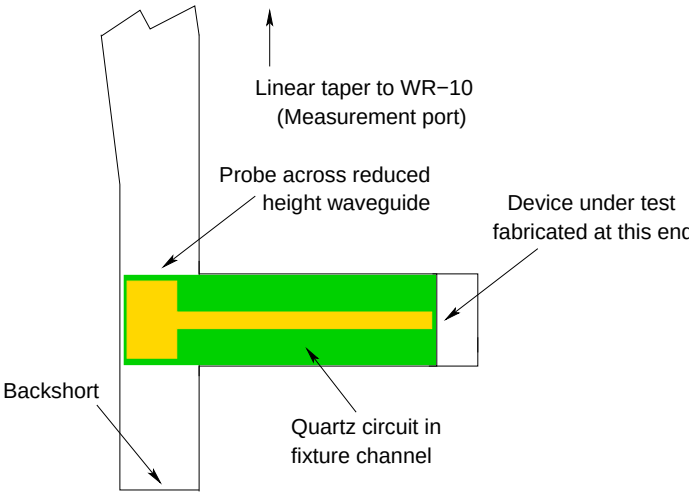

Figure 3.8: Cut away view of the test fixture, showing the placement of quartz circuit with the device under test inside.

3.5.3 Test Procedure

The test-fixture was first simulated as a two-port structure in Hewlett Packard's High Frequency Structure Simulator (HP-HFSS) [146] to evaluate its two-port S-parameters. The WR-10 waveguide flange formed one port of the simulation structure, while the cross-section of the channel where the capacitor under test was attached to the microstrip formed the other port. Knowledge of the two-port S-parameters of this part of the test-fixture along with the measured value of the reflection coefficient of the assembled fixture, allowed for the computation of the S-parameters of the device under test. This was done using the relation

$$\Gamma_{DUT} = \frac{\Gamma_M - S_{11}}{S_{21}S_{12} - S_{11}S_{22} + \Gamma_M S_{22}} \tag{3.1}$$

where, S_{ij} are the two-port S-parameters of the portion of the test-fixture excluding the device under test computed using HP-HFSS as described earlier, Γ_M is the reflection coefficient of the assembled fixture as measured by the

network analyzer, and Γ_{DUT} is the desired value of the reflection coefficient for the capacitor being evaluated (see Figure 3.9).

The actual impedance, Z_{DUT}, presented by the device was calculated by substituting Γ_{DUT} obtained above into the familiar relation

$$Z_{DUT} = 50 \left(\frac{1 + \Gamma_{DUT}}{1 - \Gamma_{DUT}} \right) \tag{3.2}$$

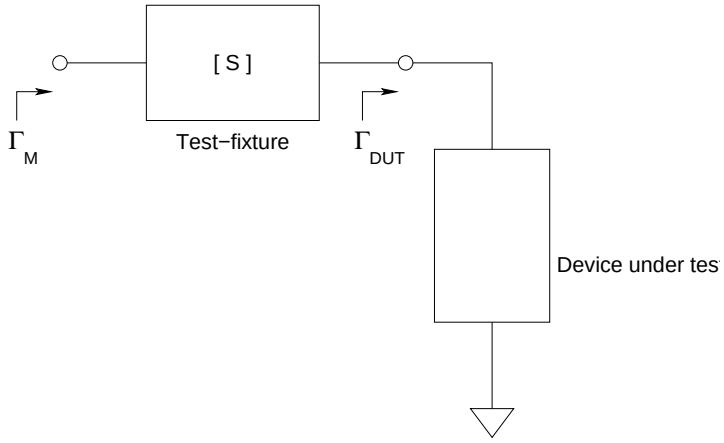

Figure 3.9: Block diagram of the experimental setup.

A "test short structure" which had the capacitor structure replaced with a short circuit was placed in the test-fixture and measured. The Z_{SHORT} for this test short, calculated by the above procedure from the measured value of Γ_{SHORT}, consisted of a $3.0 \pm 0.7\ \Omega$ real component and a small inductive component (perhaps caused by the small non-zero length of the epoxy short). This small value of Z_{SHORT} validated the de-embedding strategy used in the experiment. Furthermore, these values were recorded as a function of frequency and subsequently used to correct the impedances of the capacitors under test.

3.5.4 Measurement Results

The test devices were mounted into the fixture, one at a time, and swept frequency measurements were performed to record the reflection coefficient as a function of frequency across the entire W-Band. These were used to calculate the impedance presented by each device as a function of frequency. After application of the correction to compensate for the finite impedance of the short used to ground one end of thee device, a best fit capacitance was estimated and is presented in Table 3.1 for each type of device tested. The values of Q (corresponding to an operating frequency of 100 GHz) are listed alongside as well.

Table 3.1: Capacitance, equivalent series resistance, and Q of integrated capacitors.

Dielectric Material	Capacitance (fF)	Resistance (Ω)	Q (at 100 GHz)
Sputtered-SiO_2 Dielectric thickness, $t = 0.3\ \mu m$ Capacitor area, $A = 400\ \mu m^2$	44.4 ± 6.4	7.8 ± 1.2	4.6
Sputtered-SiO_2 Dielectric thickness, $t = 0.4\ \mu m$ Capacitor area, $A = 400\ \mu m^2$	36.2 ± 4.5	11.9 ± 3.1	3.7
CVD-SiO_2 Dielectric thickness, $t = 0.7\ \mu m$ Capacitor area, $A = 400\ \mu m^2$	26.7 ± 4.8	20.3 ± 3.2	2.9
CVD-SiO_2 Dielectric thickness, $t = 0.7\ \mu m$ Capacitor area, $A = 700\ \mu m^2$	44.9 ± 6.4	17.4 ± 4.8	2.0
SiN Dielectric thickness, $t = 0.2\ \mu m$ Capacitor area, $A = 400\ \mu m^2$	63.3 ± 3.4	3.5 ± 0.8	7.2

3.5.5 Conclusion

Inspection of the results presented in Table-3.1 reveals that irrespective of the dielectric used, the capacitors exhibited significant loss. For a fixed cross section area capacitor, the equivalent series resistance was directly proportional to the thickness of the dielectric (see measurement data for capacitors with sputter deposited SiO_2). Also, capacitors with smaller cross section area (and similar dielectric thickness) resulted in larger equivalent series resistances (see measurement data for capacitors with CVD-SiO_2), indicating that the source of the resistance was loss in the dielectric material.

For similarly sized capacitors, SiN dielectric yielded the best quality factor. Larger cross-sectional areas (often the case for DC bias bypass capacitors used on MMICs) resulted in capacitors with lower equivalent series resistance. The value of Q was however unchanged due to a corresponding change in capacitance.

The series resistance associated with the MIM integrated capacitor devices was significant for capacitor sizes likely to find application as series reactance tuning elements, even at 100 GHz. At higher frequencies these losses were only expected to get worse. Consequently the use of such capacitors was avoided altogether during the design phase of the integrated 80/240 GHz frequency multiplier in order to minimize embedding circuit losses. Instead, small gaps in microstrip transmission lines were used to synthesize series capacitive reactance tuning elements. Since the capacitance of such a structure arose out of coupling of field lines through the quartz substrate and the air gap (and not through the lossy dielectric material as was the case in the MIM structures evaluated above), the losses associated were ex-

pected to be minimal. For larger capacitor values, such as those required in RF coupling and DC bias bypass applications, the series resistance of the MIM structures should be low enough to be acceptable. Nevertheless, a novel *metal-n^--n-n^+-metal* structure [152] [153] was used for this purpose. The n^- layer with a doping level of 1×10^{16} cm^{-3} and a thickness of 0.35 μm, was designed to be completely depleted under zero bias. This resulted in a specific capacitance of 0.33 $fF/\mu m^2$. Both of these capacitor structures are explained in greater detail in the following chapter.

3.6 Integrated Inductors

Integrated inductors are required as series reactance tuning elements on a monolithic circuit. Thin spiral shaped transmission line structures, like the one illustrated in Figure-3.10, could be used to synthesize the desired inductance. In such structures, there is an associated parasitic capacitance arising out of the coupling between the adjacent conductors of the spiral and also from coupling between the spiral metalization and the bridge. In a lumped equivalent circuit, this parasitic capacitance could be modeled as an equivalent capacitor appearing in parallel with the synthesized inductance. Therefore care would have to be exercised while designing such a structure to keep the parasitic capacitance at a low value (by increasing the gap between adjacent conductors of the spiral structure), so as not to effect the synthesized inductive reactance or perhaps even resonate with it, particularly at the higher frequencies expected to be encountered in a design. Simulations carried out in HP-HFSS revealed that this was a viable approach. Also, as described below, there was good agreement between simulation and measurements performed on some test structures.

3.6.1 Test Structure and Experimental Setup

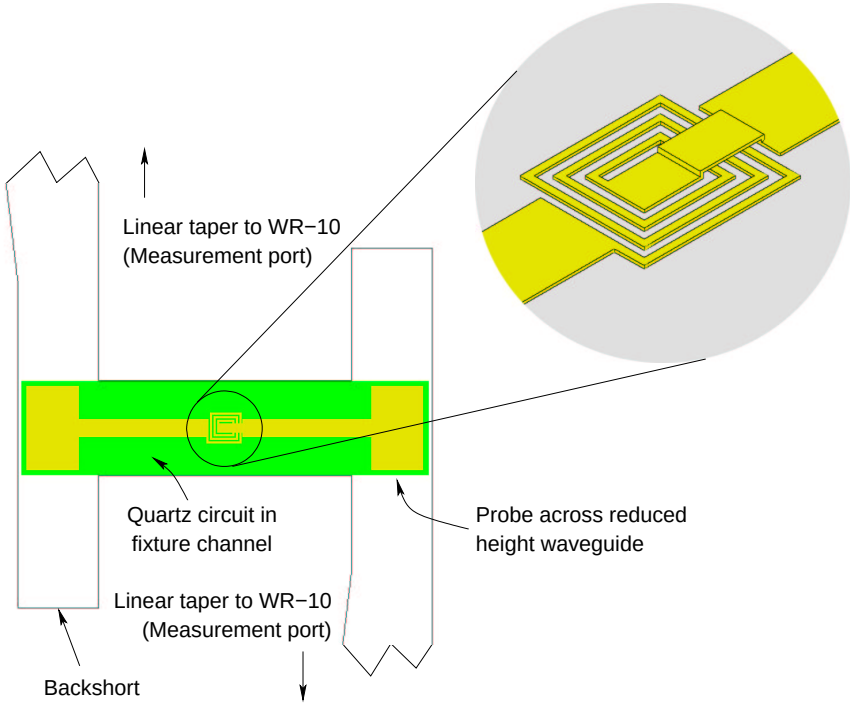

Figure 3.10: The circuit used for the evaluation of the planar integrated inductor element [154].

As in the case of integrated capacitors, evaluation was carried out on test structures in the W-Band. One port vector measurements, similar to those performed on integrated capacitors, could be performed as a function of frequency and the resulting data fitted to a parallel LC lumped element model. However this strategy was not employed, since the small value of parasitic capacitance (corresponding to a rather large capacitive reactance) could result in significant measurement error. A larger designed value of parasitic capacitance, on the other hand, would result in a structure close to anti-resonance and not suitable for accurate one port vector measurements. To get around this problem two port measurements were made. An integrated spiral induc-

tor, with an inductance value large enough to resonate with the associated parasitic capacitance within the measurement band, was designed. A comparison of the simulated and measured values of the resonance frequency, revealed by a plot of S_{21} versus frequency, was used to test the accuracy of the design. To allow for two port measurements to be made using the HP8510C Network Analyzer, a test fixture with back to back rectangular waveguide to microstrip transitions was used. As shown in Figure-3.10, the inductor structure to be evaluated was fabricated connected in between the two microstrip lines.

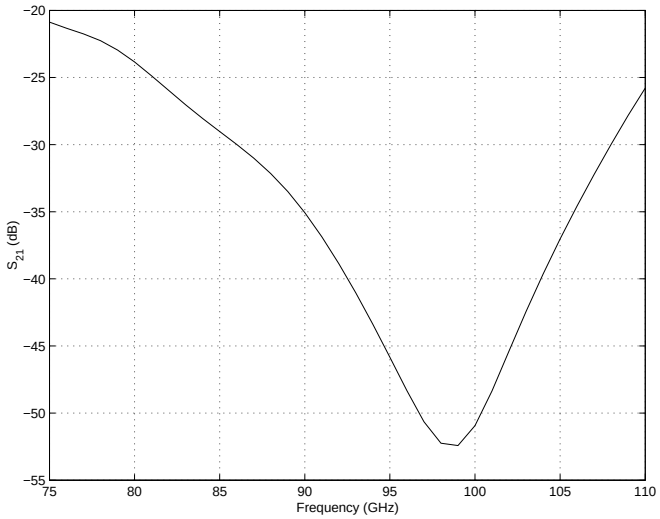

Figure 3.11: Plot of the simulated values of S_{21} for the spiral inductor structure of Figure-3.10.

3.6.2 Results

Figure-3.11 and 3.12 respectively show the simulated and measured values of S_{21} plotted versus frequency, revealing a good agreement between theory and practice.

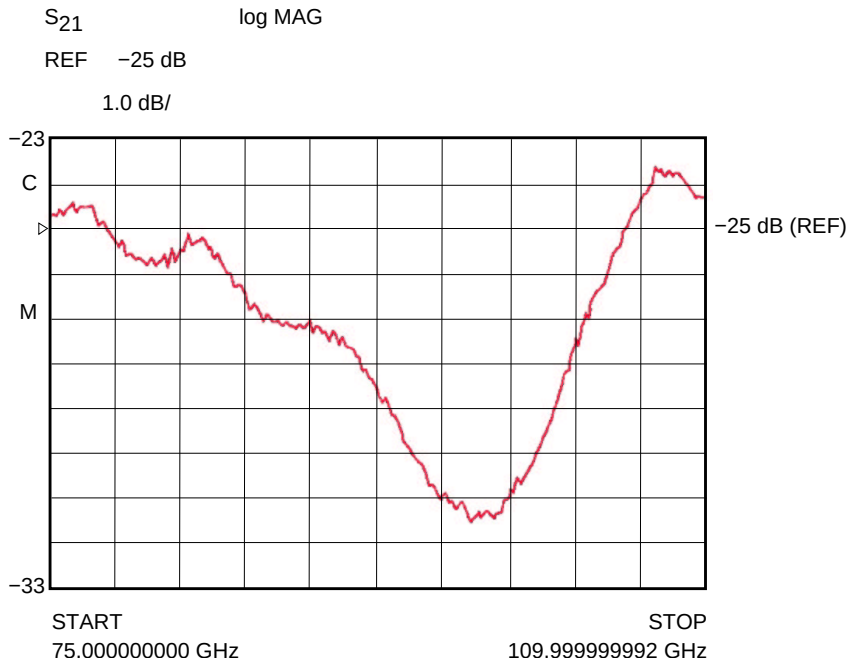

Figure 3.12: Plot of the measured values of S_{21} for the spiral inductor structure of Figure-3.10.

The null in S_{21} due to the self-resonance in the spiral inductor could possibly be exploited in some frequency multiplier designs. The spiral inductor could be used as a compact replacement for a band-stop filter circuit while simultaneously providing a series inductive tuning element at some lower frequency.

3.7 Conclusion

The design of a monolithic frequency multiplier, by definition, requires the fabrication of both the input and output linear embedding circuits together with the non linear diodes on a single piece of substrate. The benefit derived by doing this accrues from the fact that the photolithographically fabricated

embedding circuits can be realized more accurately than sections of a machined waveguide, thereby resulting in a more optimal performance. Since all of the circuit resides on a single chip, this should yield an added advantage of requiring lesser post fabrication assembly effort. There should also be the benefit of a greater repeatability of designs, being limited only by the variability of the photolithographic fabrication process.

In order to realize these benefits, suitable integrated circuit-element structures are required on the chosen substrate and material system in order to be able to perform a design. This chapter described an investigation of this requirement, and the selection of suitable circuit elements anticipated to be required for the design of a 80/240 GHz monolithic frequency tripler, which is described in the following chapter.

Chapter 4

A Fully Integrable Frequency Tripler

An 80/240 GHz frequency tripler was designed, fabricated and evaluated. The frequency tripler was designed around an "integrable" Schottky diode chip fabricated on a GaAs-membrane-on-quartz composite substrate described in Chapter-3. Details of the frequency tripler are presented in this chapter.

As will be explained later, the idler circuit was fabricated as an integral part of the diode chip. The input and output embedding networks were however fabricated separately on 1 mil thick fused-quartz substrate and con-

nected to the diode chip to complete the circuit (and yield a quasi-MMIC frequency tripler). This was done to conserve area on the diode wafer since the embedding circuits were rather large, and full integration would significantly reduce the number of devices that could be fabricated on the wafer at this proof of concept stage. Complete integration should however be quite straightforward given the fact that both the diodes and the passive linear embedding circuits are on fused-quartz substrate. This issue is addressed towards the end of the chapter.

4.1 Introduction

Like the frequency doubler, a frequency tripler is a device with two RF ports. It is designed such that when the input port is driven (or "pumped") by a source or generator at some frequency f_0, the output port delivers a third harmonic of the source at frequency $3f_0$. Just as in the case of the frequency doubler, the tripling action is brought about by the non-linear device(s) present in the circuit. The conversion efficiency of the frequency tripler, η_m, depends on several factors: The input and output embedding impedance presented to the non-linear device(s), the losses inherent in the non-linear device(s), and the losses in the input and output coupling networks. If the non-linear device(s) were lossless (such as a lossless varactor), then in the absence of any circuit losses it would be possible to achieve a conversion efficiency of 100% [138] [139] provided the input and output embedding impedances were optimally designed. Of course real world frequency triplers have device and circuit losses which tend to lower the actual realized efficiency, as was also the case with frequency doublers.

The operation of a frequency tripler, like that of a frequency doubler, is based on non-linear phenomena. Consequently the optimal embedding impedance at the source (or fundamental) frequency, as well as that at the second and third harmonic of the source frequency is a function of the input pump power. Therefore a frequency tripler should be expected to operate close to its peak efficiency only when pumped by an input power level close to the design value. For other input power levels, the optimum embedding impedances differ from the ones synthesized by the frequency tripler circuitry and consequently, the efficiency drops.

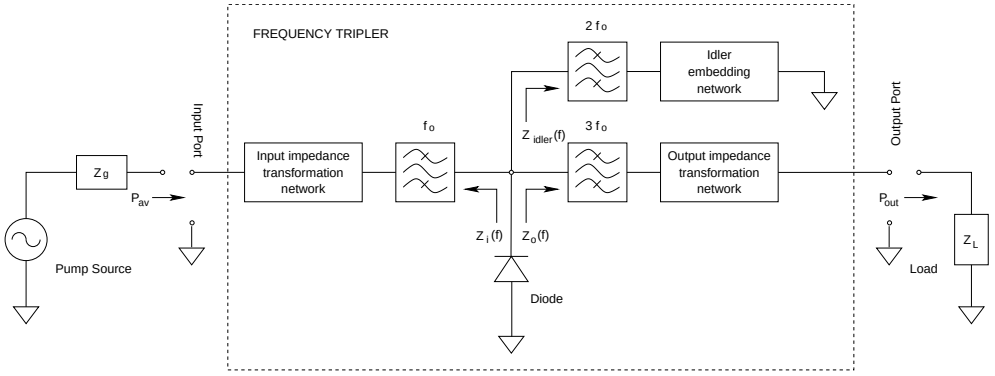

Figure 4.1: A single diode based frequency tripler.

Figure-4.1 illustrates the circuit configuration of a typical frequency tripler designed around a single diode. The input impedance matching network serves to transform the generator (source) impedance to the optimum input embedding impedance required to be presented to the diode. The output impedance matching network serves a similar purpose at the output frequency, transforming the load impedance into a value that optimizes the conversion efficiency (i.e. optimum output embedding impedance). The idler embedding network presents the optimum embedding impedance to the diode

at the second harmonic of the source frequency and provides a path for the second harmonic (or "idler") currents to circulate. The bandpass filters in the input, idler and output circuits serve to electrically isolate each circuit from the other two. Since the equivalent impedance, $Z_{emb}(f)$, presented across the diode terminals is a parallel combination of $Z_i(f)$, $Z_{idler}(f)$ and $Z_o(f)$, the filters should be designed such that $Z_i(3f_0)$, $Z_{idler}(3f_0)$, $Z_o(f_0)$, $Z_{idler}(f_0)$, $Z_i(2f_0)$ and $Z_o(2f_0)$, are as close to an open circuit as possible. This prevents the possibility of the bandpass filter in any one branch of the circuit from shunting the signal in the other two branches. Notice that the corresponding restrictions in the case of a single diode based frequency doubler of Section-2.2 were far fewer (only two). For this reason, the task of designing the embedding networks for a frequency tripler is considerably more complex than that for a frequency doubler.

4.2 An Alternate Frequency Tripler Configuration

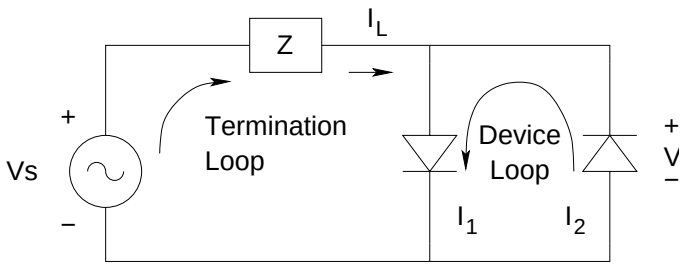

Figure 4.2: An alternate tripler circuit employing anti-parallel diode arrangement.

Figure-4.2 shows an alternate arrangement of varactor diodes that could be employed in frequency tripler designs instead of the "single-ended" diode configuration described in the previous section. The operation of such a configuration as a frequency tripler can be described as follows: The non-linear charge-voltage relationship for each of the two varactors may be represented by a power-series

$$Q(V) = a_1V + a_2V^2 + a_3V^3 + a_4V^4 + \ldots \tag{4.1}$$

where V is the voltage across the diode and $Q(V)$ is the corresponding charge stored in the device. The current through the diode can be computed from

$$I = \frac{dQ}{dt} = [a_1 + 2a_2V + 3a_3V^2 + 4a_4V^3 + \ldots]\frac{dV}{dt} \tag{4.2}$$

Thus for a voltage $V(t)$ across the diodes given by

$$V(t) = sin(k\omega_0 t) \tag{4.3}$$

the currents $I_1(t)$, $I_2(t)$ in the two loops of the circuit take the form,

$$I_1(t) = b_1cos(k\omega_0 t) + b_2sin(2k\omega_0 t) + b_3cos(3k\omega_0 t) + \ldots \tag{4.4}$$

$$I_2(t) = -b_1cos(k\omega_0 t) + b_2sin(2k\omega_0 t) - b_3cos(3k\omega_0 t) + \ldots \tag{4.5}$$

Consequently the load current, I_L, through R_L becomes

$$I_L(t) = I_1(t) - I_2(t) = c_1cos(k\omega_0 t) + c_3cos(3k\omega_0 t) + \ldots \tag{4.6}$$

which shows that only odd harmonic currents flow in the termination loop. The even harmonic currents are constrained within the device loop. Therefore a circuit configuration consisting of anti-parallel arrangement of electrically identical diodes could be used as a frequency tripler without requiring

a second harmonic bandpass filter (that was shown in Figure-4.1), thereby eliminating the associated impedance constraints discussed in Section-4.1 considerably reducing the task of designing the embedding network. The input (fundamental or source harmonic frequency) and the output (third harmonic of the source frequency) would still require bandpass filters to separate the associated signals and couple them from and to their respective waveguides, since both are odd multiplies of the source frequency and cannot be otherwise differentiated in the termination loop. This is unlike the situation encountered in designing frequency doublers where the input and output frequencies could be isolated by harmonic separation. The simplified circuit configuration to implement a frequency tripler, based on the anti-parallel diode arrangement of Figure-4.2, is presented in Figure-4.3.

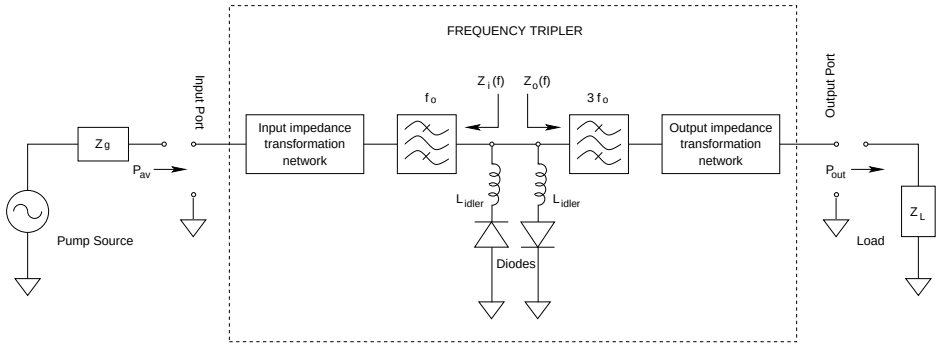

Figure 4.3: A practical frequency tripler circuit configuration based on anti-parallel arrangement of diodes.

As explained earlier, the input impedance matching network serves to transform the generator (source) impedance to the optimum input embedding impedance required to be presented to the diodes. The output impedance matching network serves a similar purpose at the output frequency, transforming the load impedance into a value that optimizes the conversion effi-

ciency (i.e. optimum output embedding impedance). The input and output filters serve to isolate the input and output ports, preventing the possibility of the input power propagating into the output port and vice-versa. Since the equivalent impedance, $Z_{emb}(f)$, presented across the diode-pair terminals is a parallel combination of $Z_i(f)$ and $Z_o(f)$, the filters should be designed such that $Z_i(3f_0)$ and $Z_o(f_0)$ are as close to an open circuit as possible. This prevents the output network from loading the input circuit or the input network from shunting the third harmonic signal (which represents the useful output of the frequency tripler). The inductance of the Schottky contact bridge metalization, represented by inductors of value L_{idler} in series with each diode in the figure, is designed to present the desired inductive reactance in the idler loop. The two inductors appear in series for the idler currents. The input and output circuits also need to be designed to take into account the effect of these inductors which appear in parallel for odd harmonic currents.

The 80/240 GHz frequency tripler, described next, was based on this circuit configuration.

4.3 The 80/240 GHz Frequency Tripler

The input of the frequency tripler was a standard WR-12 (E-Band) rectangular waveguide. The height was tapered down to a quarter height to allow for the design of a broadband waveguide to microstrip coupler that provided the pump power to the rest of the input embedding network. Similarly, the output embedding network terminated in a microstrip to waveguide probe that coupled power into a half height WR-4 waveguide. As before, the coupler was designed into a reduced height waveguide to maximize the useful bandwidth

of the coupler. The height was subsequently tapered up to full height and a standard WR-4 rectangular waveguide section formed the output flange of the frequency tripler. Figure-4.4 shows the placement of various components used in this frequency tripler. The relative placement of the input and output circuits with respect to the integrated diode chip in the actual frequency tripler block can be found in Figure-E.5.

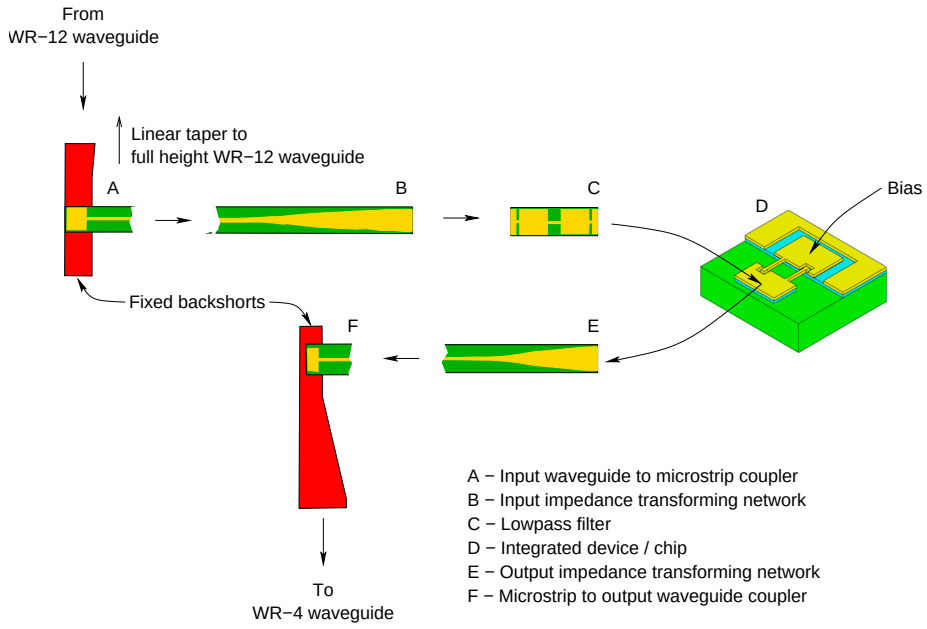

Figure 4.4: Relative placement of various components used in the 80/240 GHz frequency tripler.

Since the WR-4 output waveguide is cut-off at input frequencies, the output bandpass filter of Figure-4.3 was not required. However, the output network was still required to meet the condition that $Z_o(f_0)$ be close to an open circuit to avoid loading the input circuit for reasons explained earlier. With the idler frequency being decoupled from the input circuit due to harmonic separation the bandpass filter in the input circuit of Figure-4.3 was

replaced by a simpler lowpass filter as shown and prevented the coupling of the third harmonic output signal into the input waveguide. The input and output impedance transforming networks were designed to present the optimum embedding impedances to the integrated chip at their respective frequencies.

The design of the integrated chip as well as the input and output embedding circuits are discussed in the following sections.

4.4 Design of the Integrated Device

The integrated chip, previously described in Section-3.2, consisted of two anti-parallel Schottky diodes with an air bridge geometry that was optimized to synthesize the desired inductance for the idler loop. An integrated DC bias bypass capacitor, as shown in Figure-4.5, was also included to allow for the reverse biasing of the two Schottky diodes in series, while still providing a path for the RF currents.

4.4.1 The DC Bias Bypass Capacitor

The DC bias bypass capacitor was realized as a *metal*-n^--n-n^+-*metal* structure. The n^- layer, with a doping level of 1×10^{16} cm^{-3} and a thickness of 0.35 μm, was designed to be completely depleted under zero bias. This resulted in a specific capacitance of 0.33 $fF/\mu m^2$. Application of a negative bias on the capacitors' top pad metalization would result in an additional depletion of the underlying epitaxial layer. One of the criteria used to select the doping concentration for the epitaxial layer was to ensure that application of

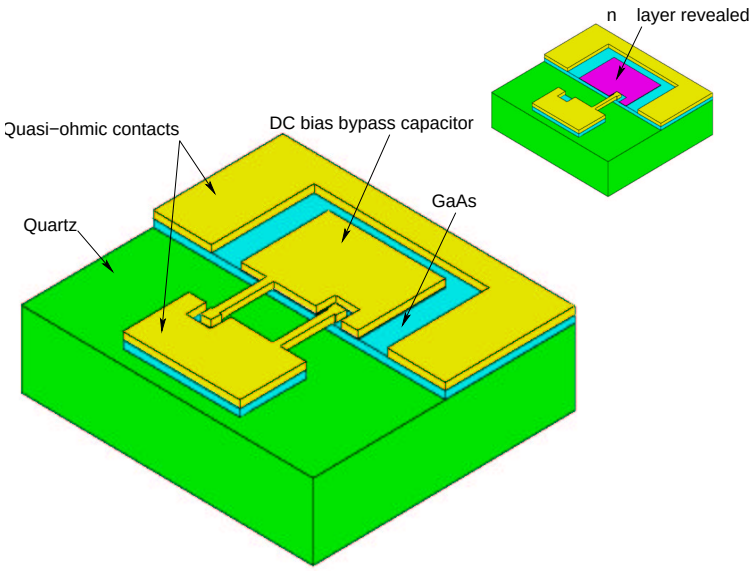

Figure 4.5: Layout of the quartz based integrated device, consisting of two Schottky diodes in an anti-parallel configuration and a large capacitor to accommodate the DC bias arrangement. The smaller inset is a view with the top metalization of capacitor removed to reveal the n^- layer underneath.

bias did not result in an excessive modulation of the bias capacitance. Furthermore, the size of this capacitor structure was chosen to be large enough (the actual capacitor had an area of 4800 μm^2) so as to ensure a low capacitive reactance at the lowest frequency of operation. For the selected epitaxial layer doping level of 2×10^{17} cm^{-3}, the reactance of the bias capacitor was expected to be under $-j1.5\ \Omega$ at 80 GHz for a maximum expected instantaneous reverse bias of 20 V, corresponding to a depletion width of 0.16 μm in the epitaxial layer.

4.4.2 Determination of Primary Design Parameters

As a step towards designing the integrated chip for the 80/240 GHz frequency tripler, the primary design parameters needed to be determined. Specifically, the desired doping levels for the buffer layer and epitaxial layer (N_{buffer} and N_d respectively) were to be ascertained. Also, the optimum buffer layer thickness, t_{buffer}, and the optimum epitaxial layer thickness, t_{epi}, were to be selected. The process of selecting these parameters is addressed in the following paragraphs.

As was done in the case of frequency doublers in Chapter-2, buffer layer doping levels close to 10^{18} cm^{-3} and epitaxial layer doping levels in the range from 10^{16} cm^{-3} to 10^{17} cm^{-3} were studied to identify their optimum values. As a starting point, the data in Figure-2.9 (reproduced in Figure-4.6 here) was used to select the buffer layer doping level, N_{buffer}, and its thickness, t_{buffer}.

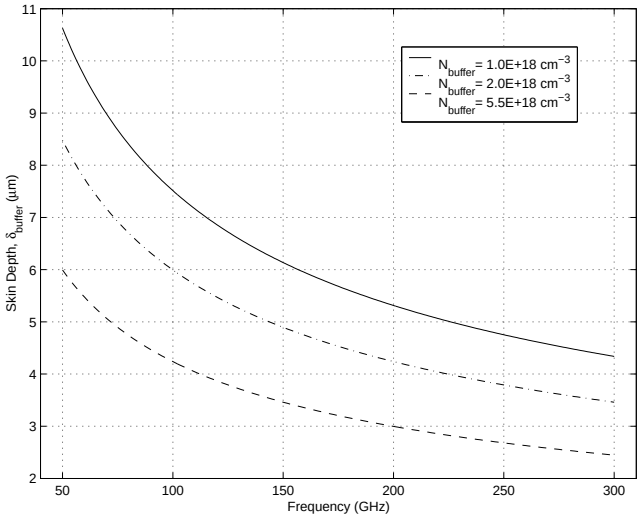

Figure 4.6: Plot of skin depth in the buffer layer vs. frequency for three doping levels.

Since the larger skin depths occur at lower frequencies, the choice of the buffer layer thickness and doping level was based on the lowest frequency of operation (i.e. the tripler input frequency of 80 GHz). In order to minimize the series parasitic resistance, the buffer layer doping was be chosen to be as high as possible. $N_{buffer} = 5.5 \times 10^{18}\ cm^{-3}$ was selected because it represents the upper limit of doping level in commercially available material systems. The thickness of the buffer layer, t_{buffer}, was chosen to be 5 μm to satisfy the condition that the maximum skin depth (4.7 μm at 80 GHz from Figure-4.6) be smaller than the buffer layer thickness.

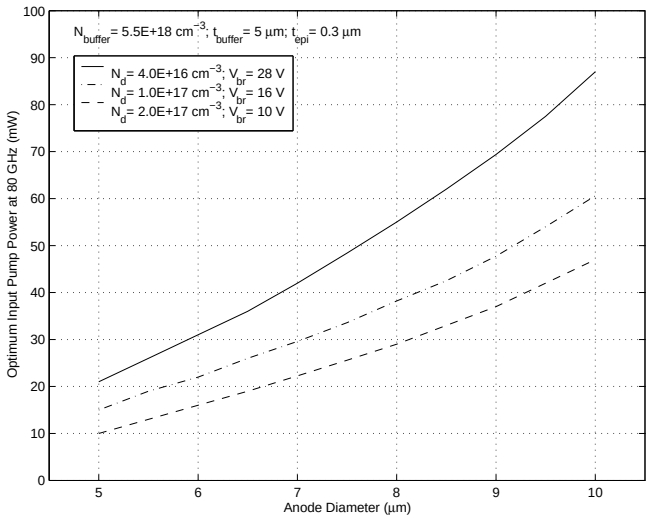

Figure 4.7: Input power (per diode) to obtain maximum conversion efficiency, for different anode sizes and epitaxial layer doping level.

The choice of the epitaxial layer thickness and doping level was dependent on the desired input pump power handling capability as well as the number and size of the junctions. Figure-4.7 shows the input power levels required to maximize the conversion efficiency for a range of anode sizes and for three available epitaxial layer doping levels under consideration. These results

were obtained from one-tone harmonic balance simulations, performed using Hewlett Packard's Microwave and RF Design System (MDS) [145], for a single diode presented with optimum input, idler and output embedding impedances and pumped at an input frequency of 80 GHz. The diode model that was used included only the parasitic series resistance (as calculated from Equation-2.13), and the zero bias junction capacitance (as calculated from Equation-2.12). The reverse breakdown voltages used in these calculations were obtained from Figure-2.6.

The frequency tripler was intended to be pumped by a Gunn-diode based oscillator that had an output of about 50 mW. Since the integrated device was to consist of two diodes, a power handling capability of 25 mW/anode was required. From the data in Figure-4.7, it is evident that any of the three epitaxial layer doping level values could meet this requirement with an appropriate choice of anode size.

Another factor that was considered while making a choice for the epitaxial layer doping level was the phenomenon of electron velocity saturation in GaAs. Most harmonic balance simulators assume an average electron velocity, $\vec{v}_e$, to be proportional to the applied electric field, $\vec{E}$, as given by the relation

$$\vec{v}_e = \mu_e \vec{E} \tag{4.7}$$

where μ_e is the low field electron mobility. For GaAs this relation is valid for electric field strengths upto about $3.3 \times 10^5\ V/m$. For larger field strengths, the average electron velocity rolls off and subsequently drops [156]. The maximum average velocity of the electrons is termed as the electron saturation velocity, denoted by v_{sat}. Velocity saturation places an upper limit on the

peak value of current, I_{max}, in a varactor as given by

$$I_{max} = qN_dAv_{sat} \tag{4.8}$$

where N_d represents the doping concentration of the epitaxial layer and A the area of the Schottky junction. From Equation-4.7, and the maximum field strength given above, the saturation velocity of electrons may be computed using

$$v_{sat} = 3.3 \times 10^5 \mu_e \tag{4.9}$$

Equation-4.8 therefore becomes

$$I_{max} = 3.3 \times 10^5 qN_dA\mu_e \tag{4.10}$$

The electron mobility, μ_e, in GaAs decreases with an increase in donor impurity concentration. However this dependence is rather weak and the factor N_d in Equation-4.10 more than makes up for the decrease in carrier mobility due to an increase in doping concentration. Consequently, higher epitaxial layer doping concentration levels result in larger values of I_{max}. For instance, the electron mobility in GaAs with $N_d = 2 \times 10^{17}\ cm^{-3}$ is about 75% of the electron mobility in GaAs with $N_d = 1 \times 10^{17}\ cm^{-3}$ [156]. Therefore, for a given anode size, the peak value of varactor current in a diode with $N_d = 2 \times 10^{17}\ cm^{-3}$ would be $(2 \times 0.75 =)$ 1.5 times the peak value of varactor current in the diode with $N_d = 1 \times 10^{17}\ cm^{-3}$.

For high frequency operation of varactor diodes, the depletion region boundaries (and hence the electrons) need to move at correspondingly high velocities. Any limit on the velocity of modulation could be detrimental to the operation of the device and result in degraded performance. In light

of the above argument, the highest practical epitaxial doping level, N_d, of $2 \times 10^{17}\ cm^{-3}$ was selected.

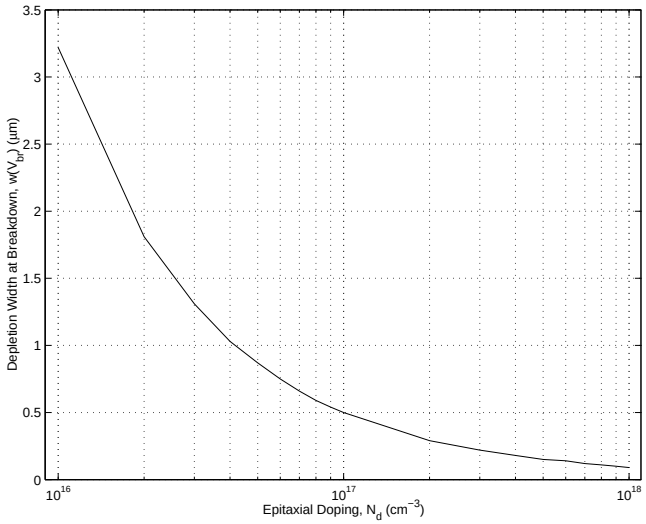

Figure 4.8: Variation of the width of the depleted region in the epitaxial layer at before breakdown as a function of epitaxial doping level.

The epitaxial layer thickness was required to be as small as possible but larger than the maximum width of the depletion layer in order to avoid punch-through. Inspection of the depletion region widths at breakdown in Figure-2.12 (reproduced here as Figure-4.8) led to the choice of $t_{epi} = 0.3\ \mu m$.

4.4.3 Design of the Planar Diode Chip

Having obtained the specifications for the material system, the next step in the design of the planar diode chip was the determination of the anode size. This was done with the aid of the data presented in Figure-4.7 in conjunction with the optimum embedding impedance data (corresponding to the selected epitaxial layer doping level, $N_d = 2 \times 10^{17}\ cm^{-3}$ and thickness, $t_{epi} = 0.3\ \mu m$) presented in Figure-4.9.

Inspection of these curves reveals that diodes with anode size of about 7.5 μm could easily meet the desired power handling capability of 25 mW/anode, while requiring reasonable embedding impedances.

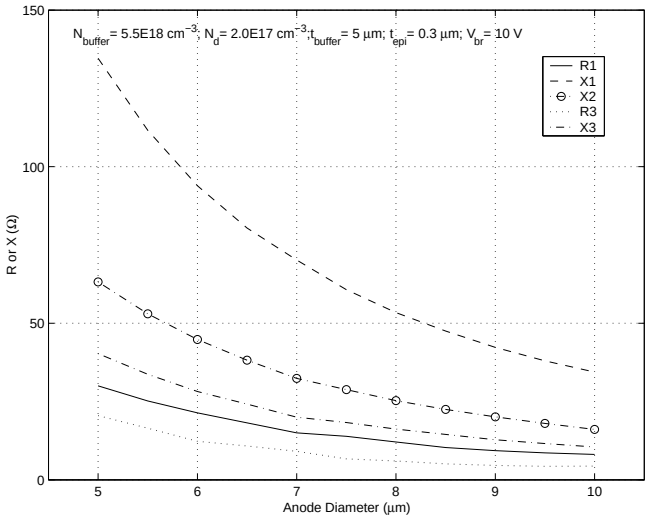

Figure 4.9: Optimum embedding impedances as a function of anode size.

The next step was to use Hewlett Packard's High Frequency Structure Simulator (HP-HFSS) [146] to optimize the air bridge geometry to synthesize the desired idler inductance as per the data is Figure-4.9. The length and width of the bridge metalization as well as the distance between the two air bridges was adjusted to complete this optimization.

Nine variations of the circuit corresponding to anode diameters of 6 μm, 7 μm, 8 μm and bridge lengths of 30 μm, 35 μm, 40 μm were fabricated. The design corresponding to the middle value of each parameter (7 μm anode diameter and 35 μm bridge length) represented the nominal design. The diodes on this chip had a calculated parasitic series resistance, R_s, of 1 Ω and were designed to have a zero bias junction capacitance, C_{j0}, of 54 fF. The reverse breakdown voltage was expected to be 10 V per anode. The overall chip dimensions were 200 $\mu m \times 180$ $\mu m \times 2$ mil.

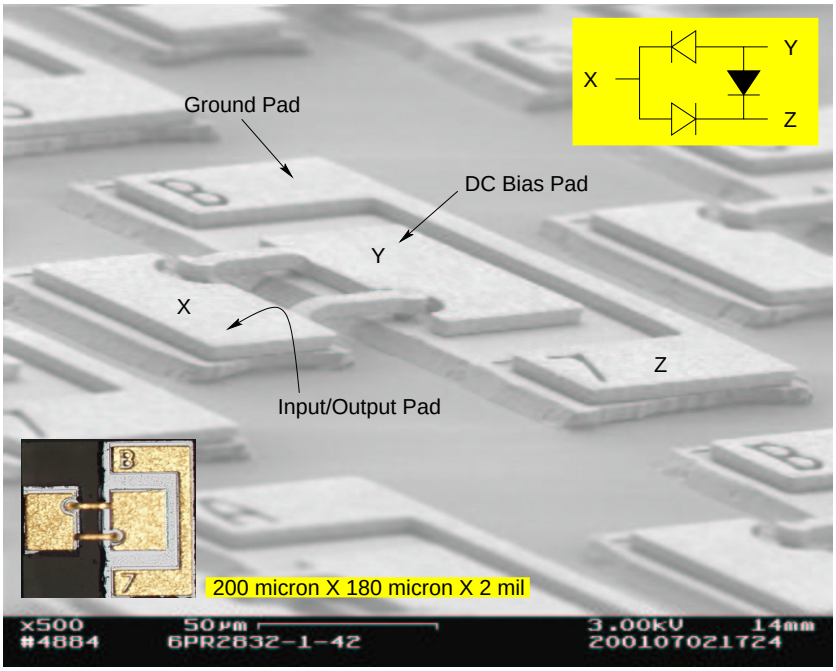

Figure 4.10: A Scanning Electron Micrograph of a completed wafer of the quartz based integrated devices, prior to the dicing operation. The location of some significant terminals is identified. The "open" diode symbols represent Schottky contacts, while the black filled diode symbol represents the location of the DC bias bypass capacitor. A photograph of a diced chip together with its dimensions is included at the bottom. Photograph courtesy Gerhard S. Schoenthal, University of Virginia, Semiconductor Development Laboratory. See also Figure-3.1.

4.5 Linear Embedding Circuit Design

In this section the process used to design the linear embedding circuit for the 80/240 GHz frequency tripler is described. The embedding circuit was implemented as a planar input and output quartz circuits (to which the planar diode chip was connected) seated in a metal mount. As was done in

the case of frequency doubler design, all the modeling and simulations were carried out using HP-HFSS and MDS.

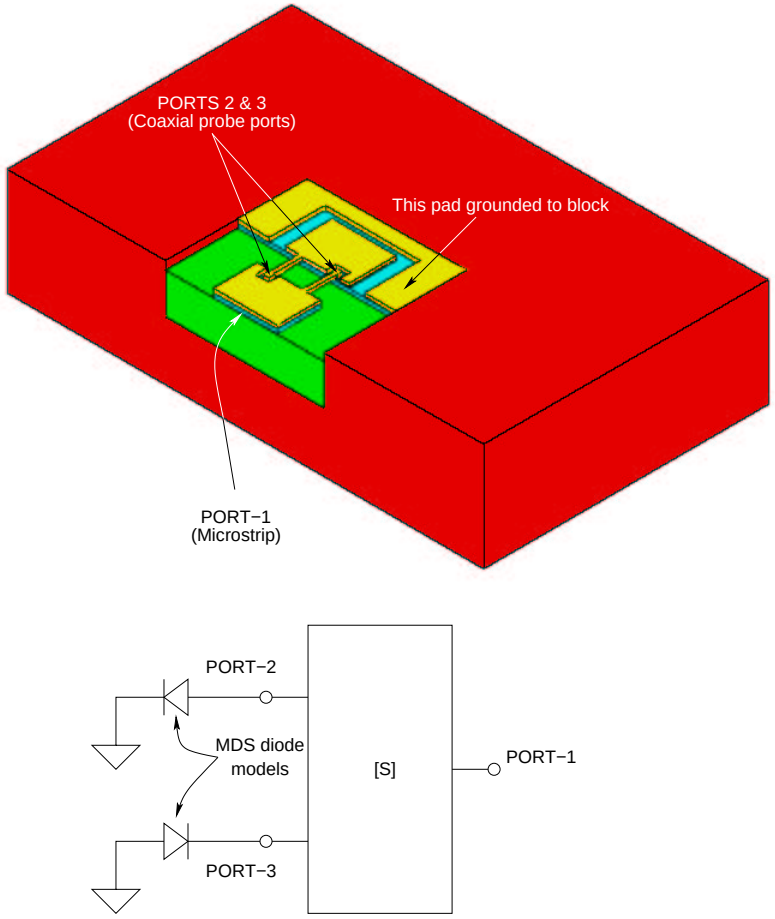

Figure 4.11: Cut away view of the structure analyzed in HP-HFSS to compute the S-parameters of the frequency tripler chip. Only bottom half of the mount that seats the diode chip is shown. Also shown at the bottom is the equivalent circuit model schematic (based on the calculated S-parameters) used in MDS to perform harmonic balance simulations to calculate the optimum input and output embedding impedances. For simplicity, the DC bias arrangement has been omitted and is not shown.

The first step was to determine the optimum input and output embedding impedances for the integrated diode chip as a whole. HP-HFSS was used to to calculate the three-port S-parameters for the chip seated in a metal block as illustrated in Figure-4.11. Coaxial probes, as described in Chapter-2, were used to attach ports at the location of the two Schottky junctions. The calculated S-parameter model was then used to define an equivalent circuit schematic model for the chip in MDS. Subsequently, one-tone harmonic balance simulations were performed after attaching diode models at the ports corresponding to the Schottky junction locations to compute the optimum input and output embedding impedances for the chip. Linear input and output circuits were then synthesized to complete the design process.

4.5.1 Design of the Input Circuit

The input circuit configuration is illustrated in Figure-4.12. The input to the frequency tripler was to be from a WR-12 (E-Band) waveguide. This full height input waveguide was tapered down to a quarter height section and a waveguide probe was located in this quarter height section to couple power into a microstrip with 50 Ω characteristic impedance. A Klopfenstein [157] type impedance taper followed by a lowpass filter constituted the remaining portion of the input circuit. The diode chip was connected to the output of the lowpass filter. The synthesis of each of the above input circuit components is described next.

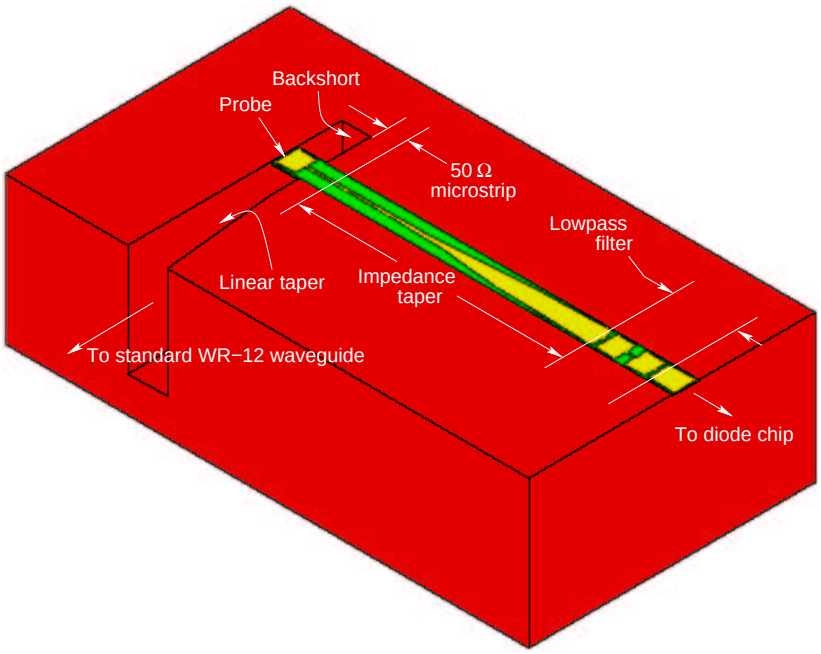

Figure 4.12: The input embedding circuit consisting of a waveguide to microstrip transition, a microstrip impedance taper and a lowpass filter. Only the bottom part of the mount that seats the quartz circuit is shown.

The Input Waveguide Taper

As stated earlier, a linear taper was employed to transition from full height waveguide to a quarter height section. The linear taper was optimized to yield a good input match (return loss of about 20 dB) for the smallest possible length of the taper section. This involved performing a series of simulations in HP-HFSS with different lengths for the taper section and selecting the shortest taper length meeting this criteria. Figure-4.13 shows S_{11} for the chosen taper length.

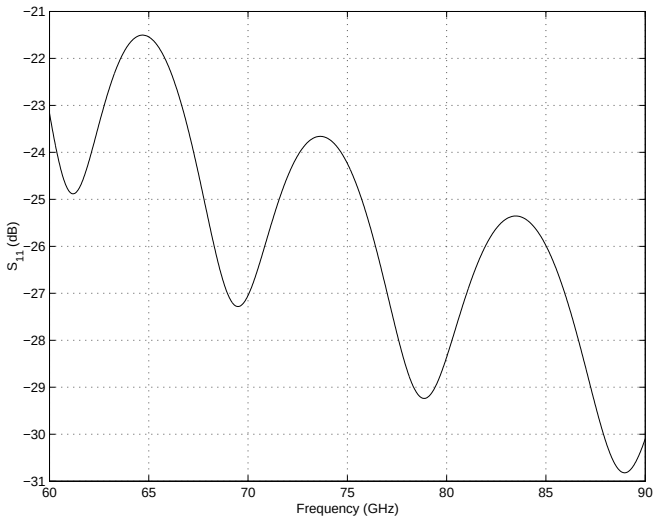

Figure 4.13: Plot of S_{11} for the WR-12 one-fourth to full height waveguide linear taper (simulated).

The Input Waveguide to Microstrip Coupler

Figure-4.14 illustrates the design of the waveguide to microstrip coupler together with the geometric parameters that were optimized in HP-HFSS and MDS to execute this design. Figure-4.15 and 4.16 respectively show the resulting S_{11} and S_{21} for the completed design.

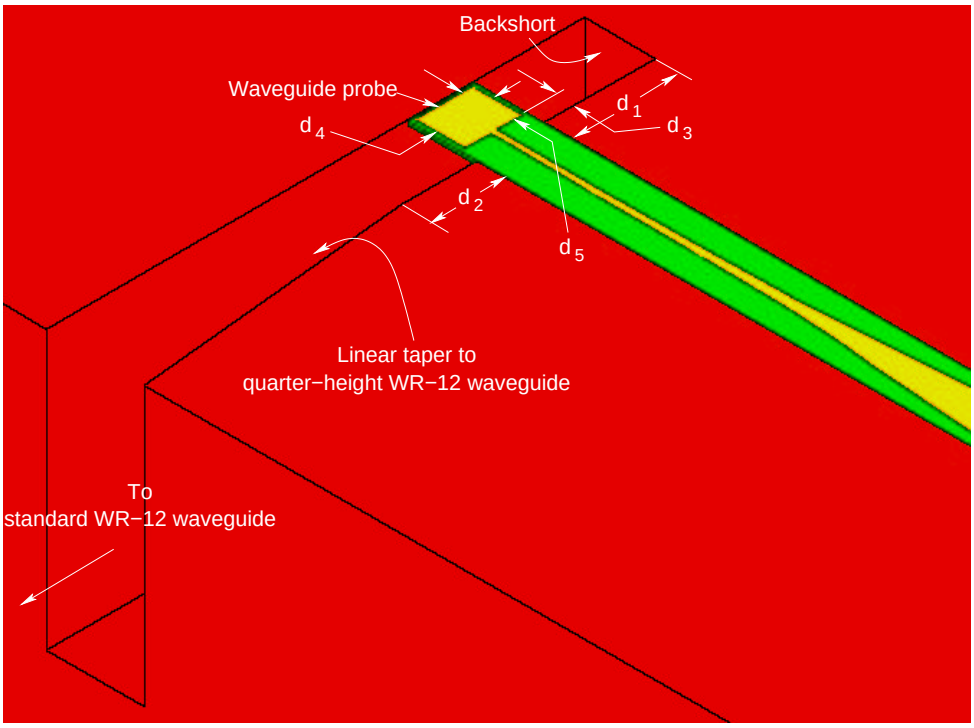

Figure 4.14: Design of the input coupler for the 80/240 GHz frequency tripler. Only bottom part of the mount that seats the quartz circuit is shown. The dimensions that were optimized to achieve a good coupling efficiency are marked.

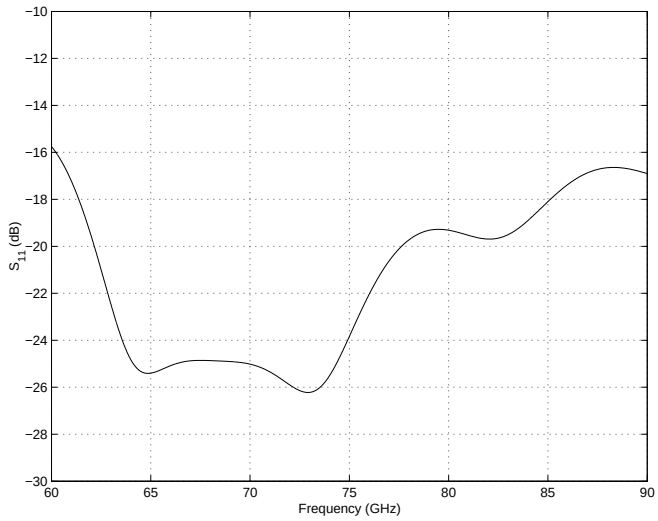

Figure 4.15: Plot of S_{11} for the input WR-12 waveguide to 50 Ω microstrip transition (simulated).

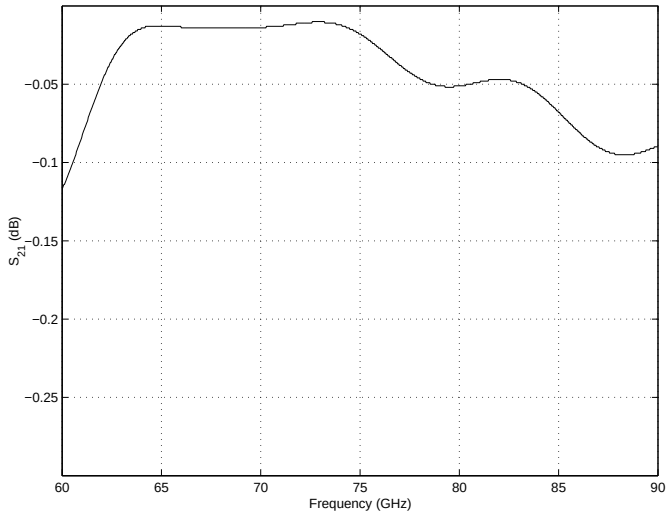

Figure 4.16: Plot of S_{21} for the input WR-12 waveguide to 50 Ω microstrip transition (simulated).

The Input Lowpass Filter

As described earlier, the function of the lowpass filter was to prevent any propagation of the third harmonic power generated in the diodes from propagating towards the input waveguide. The lowpass filter design was based on a series of cascaded microstrip transmission line sections having alternating high characteristic impedance and low characteristic impedances. Figure-4.17 illustrates the various dimensions that were optimized in HP-HFSS. Figure-4.18 has a plot of S_{21} for the resulting design.

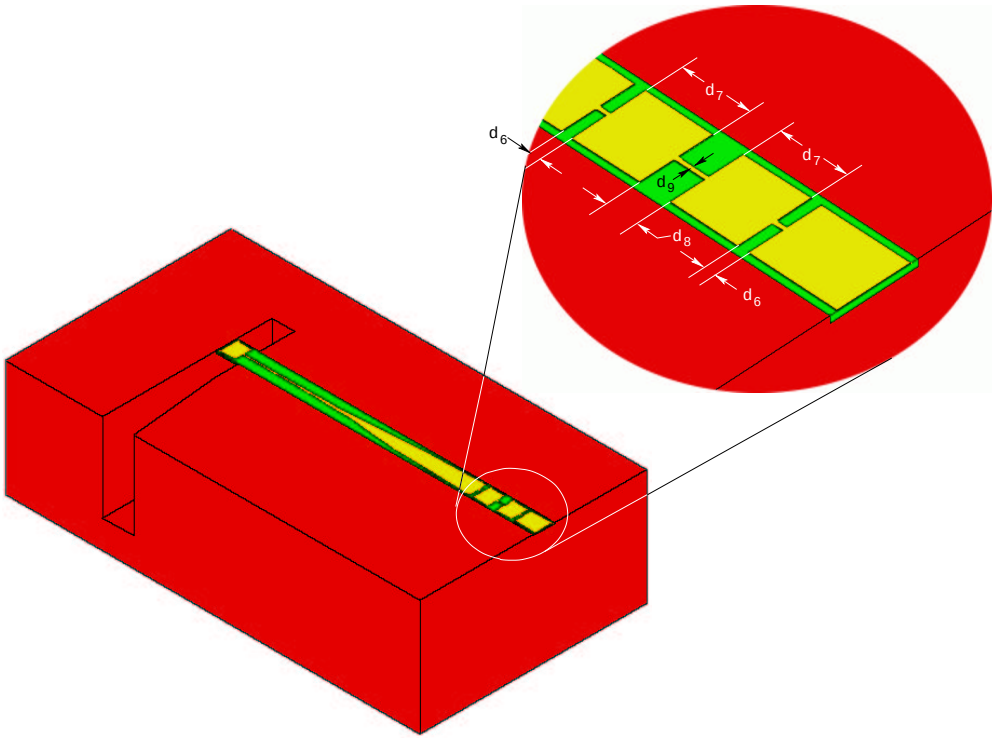

Figure 4.17: Design of the input lowpass filter. Only bottom part of the mount that seats the quartz circuit is shown. All the dimensions that were optimized are marked.

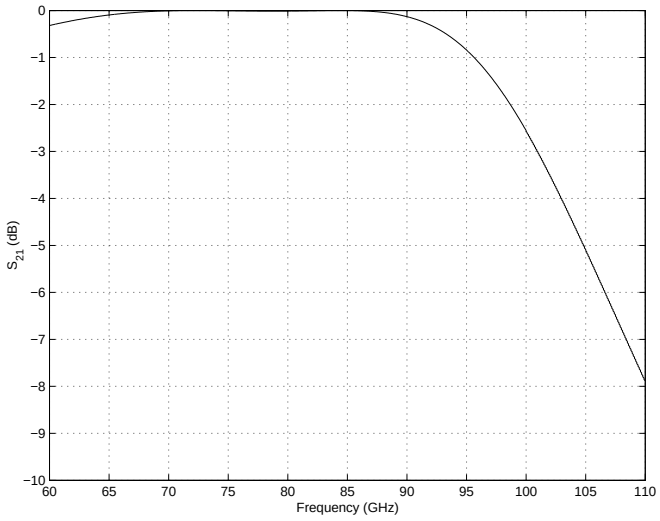

Figure 4.18: Plot of S_{21} for the input lowpass filter (simulated).

Figure-4.19 shows the complete input quartz circuit placed in the metal housing. The length d_{10} was optimized such that the impedance presented to the diode chip was close to an open circuit at the output frequency of 240 GHz. Figure-4.20 and 4.21 show the resulting S_{11} and S_{21}, respectively, for the complete input circuit.

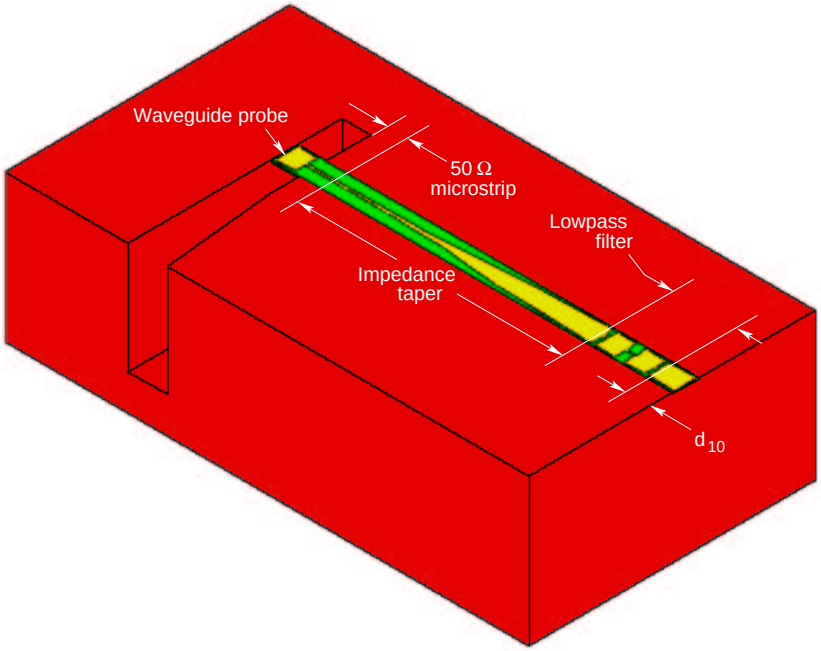

Figure 4.19: The complete input embedding circuit consisting of a waveguide to microstrip transition, a microstrip impedance taper and a lowpass filter. Only the bottom part of the mount that seats the quartz circuit is shown. The length of the section marked d_{10} was optimized such that the impedance presented to the diode chip was close to an open circuit at the output frequency of 240 GHz.

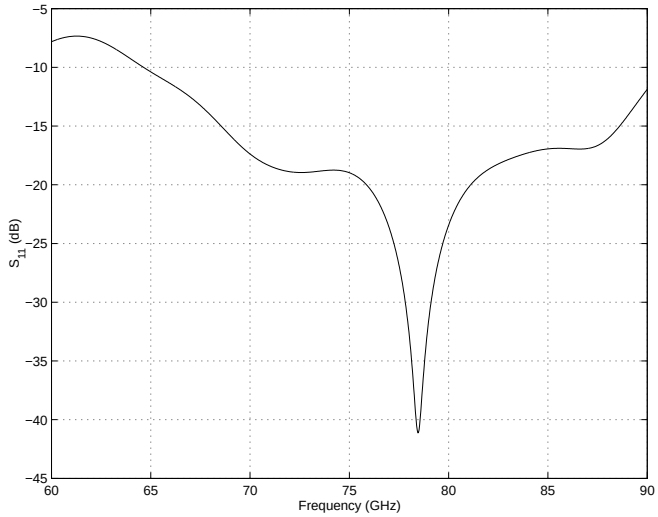

Figure 4.20: Plot of S_{11} for the complete 80/240 GHz frequency tripler input circuit (simulated).

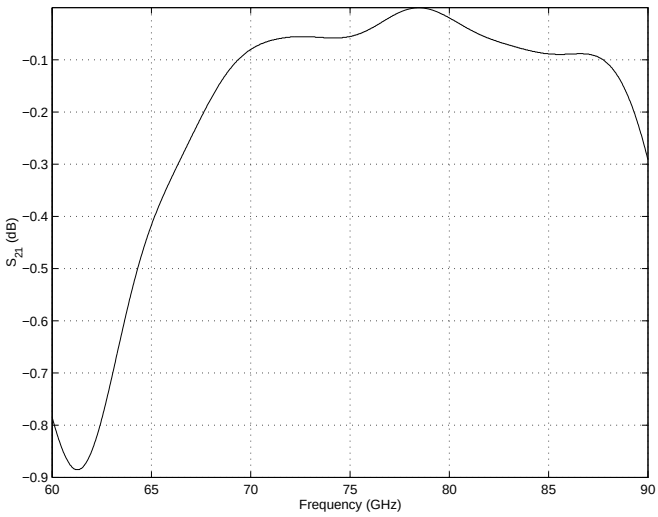

Figure 4.21: Plot of S_{21} for the complete 80/240 GHz frequency tripler input circuit (simulated).

4.5.2 Design of the Output Circuit

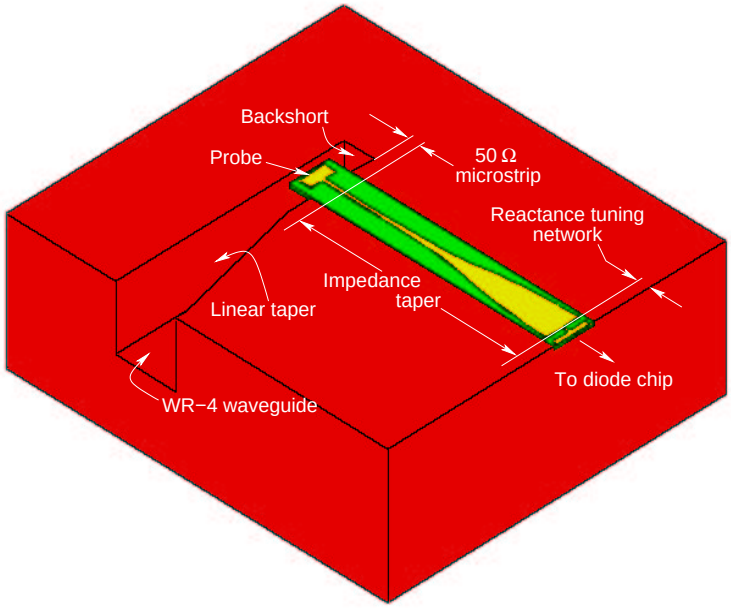

Figure 4.22: The output embedding circuit consisting of a microstrip impedance taper and a microstrip to waveguide transition. Only the bottom part of the mount that seats the quartz circuit is shown.

The output circuit configuration is shown in Figure-4.22. It consisted of a reactance tuning network followed by a Klopfenstein type impedance taper terminating in a 50 Ω microstrip. The output of the frequency tripler was to be a WR-4 waveguide. A microstrip to waveguide coupler was required for this purpose. The probe for this coupler was located in a half height section of the waveguide that was subsequently tapered up to a full height WR-4 waveguide. The diode chip was connected to the reactance tuning network end of the circuit. The output coupler was designed first, followed by the microstrip impedance taper. Finally the reactance tuning structure

was added at the low impedance end of the microstrip impedance taper. The details of the synthesis procedure for each of the above circuit components, are described next.

The Output Waveguide Taper

A linear taper was employed to transition from half height waveguide to full height waveguide. The linear taper was optimized to yield a good input match (return loss of about 20 dB) for the smallest possible length of the taper section. This involved performing a series of simulations in HP-HFSS with different lengths for the taper section and selecting the shortest taper length meeting the above criteria. Figure-4.23 shows S_{11} for the chosen taper length.

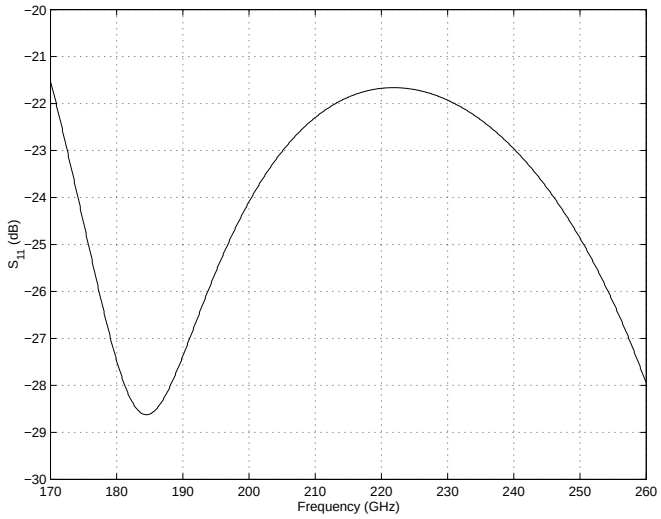

Figure 4.23: Plot of S_{11} for the WR-4 half height to full height waveguide linear taper (simulated).

The Output Microstrip to Waveguide Coupler

Figure-4.24 illustrates the design of the microstrip to waveguide coupler together with the geometric parameters that were optimized in HP-HFSS and MDS to execute this design. Figure-4.25 and 4.26 respectively show the resulting S_{11} and S_{21} for the completed design.

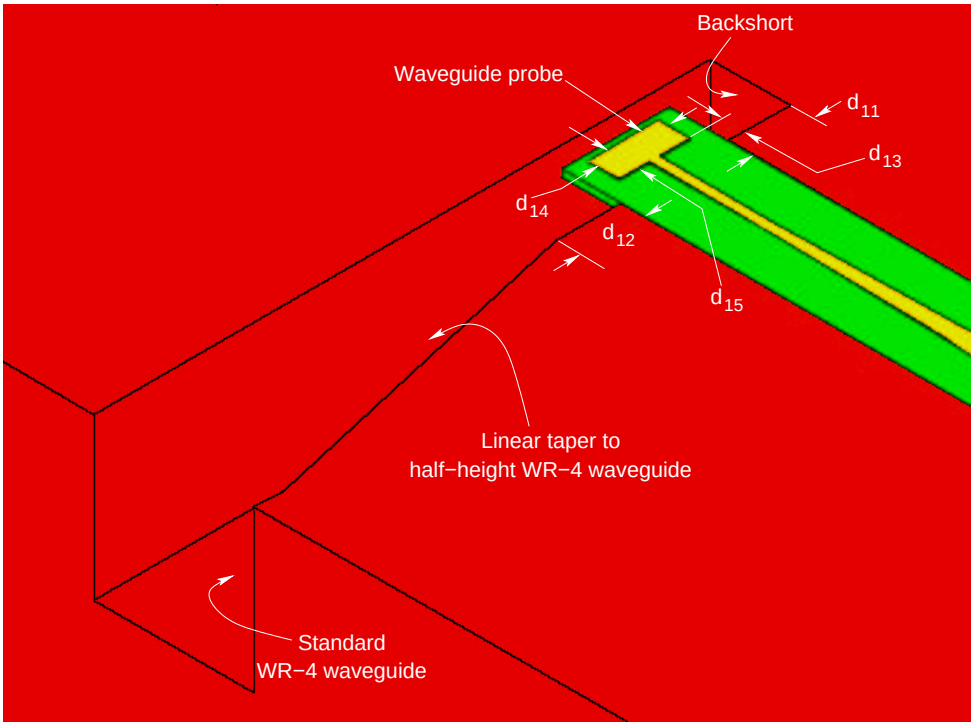

Figure 4.24: Design of the output coupler for the 80/240 GHz frequency tripler. Only bottom part of the mount that seats the quartz circuit is shown. The dimensions that were optimized to achieve a good coupling efficiency are marked.

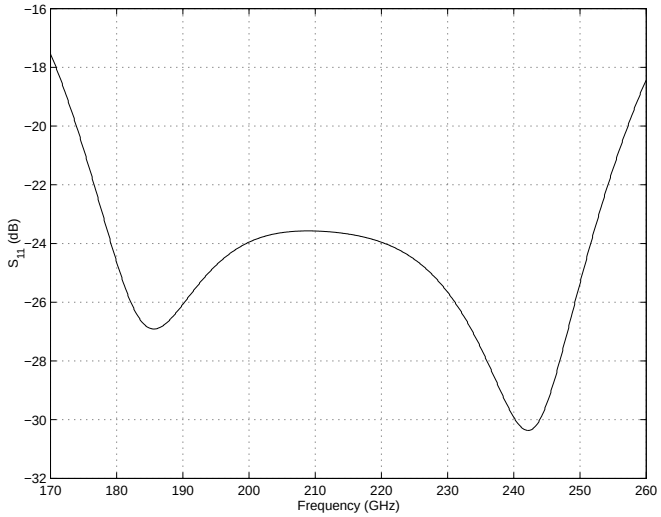

Figure 4.25: Plot of S_{11} for the output 50 Ω microstrip to WR-4 waveguide transition (simulated).

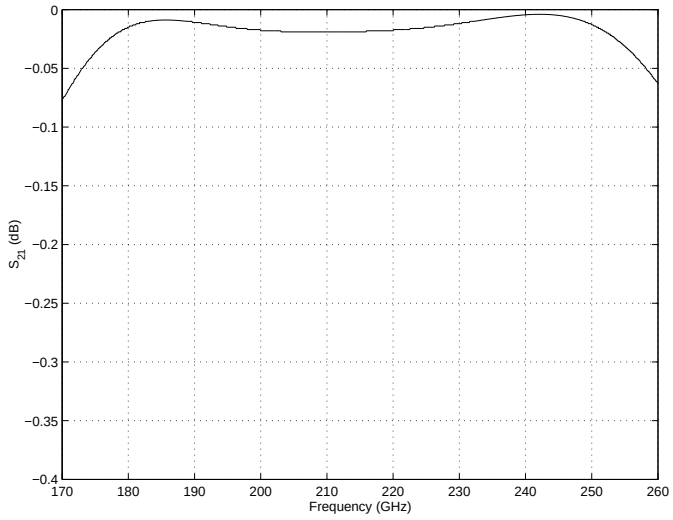

Figure 4.26: Plot of S_{21} for the output 50 Ω microstrip to WR-4 waveguide transition (simulated).

Figure-4.27 shows the complete output quartz circuit placed in the metal housing. The dimensions d_{16}, d_{17} and d_{18} were optimized to synthesize the desired reactance at the output frequency of 240 GHz. The length d_{19} was also optimized such that, at the input frequency of 80 GHz, the impedance of the cutoff WR-4 output waveguide transformed to an open circuit at the diode chip terminal. Figure-4.28 and 4.29 respectively show the resulting S_{11} and S_{21} for the complete output circuit (without the reactance tuning network).

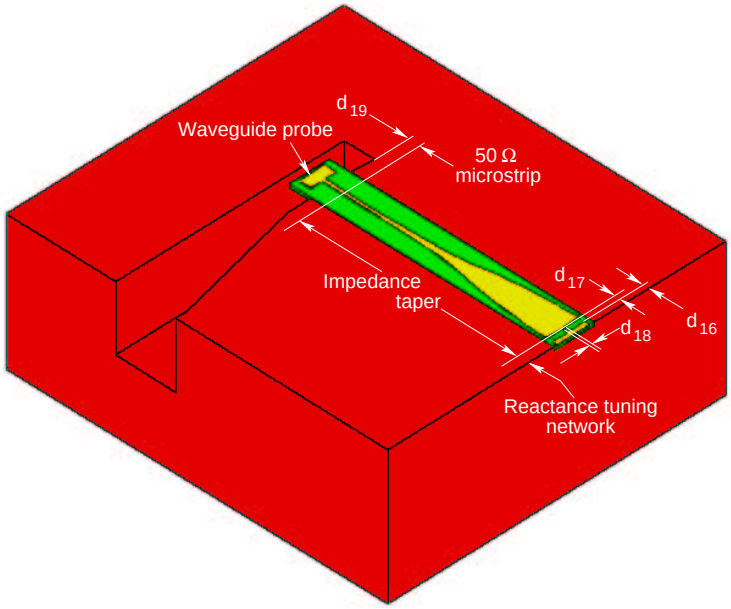

Figure 4.27: The output embedding circuit consisting of a reactance tuning structure followed by a microstrip impedance taper and a microstrip to waveguide transition. Only the bottom part of the mount that seats the quartz circuit is shown. The length of the section marked d_{16} was optimized such that the impedance presented to the diode chip was close to an open circuit at the input frequency of 80 GHz.

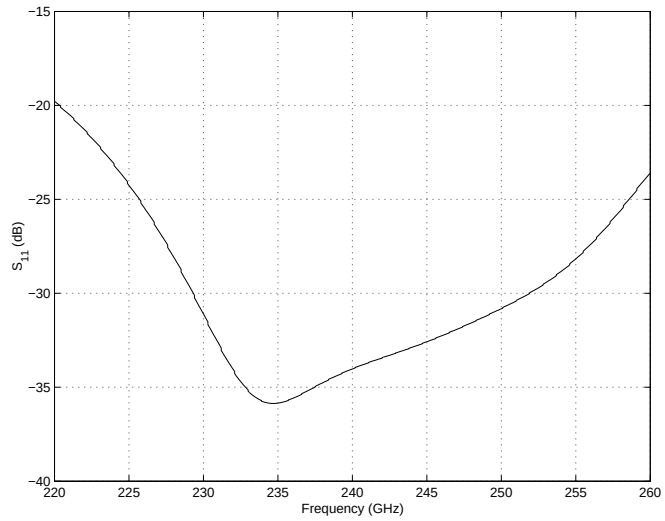

Figure 4.28: Plot of S_{11} for the complete 80/240 GHz frequency tripler output circuit (simulated).

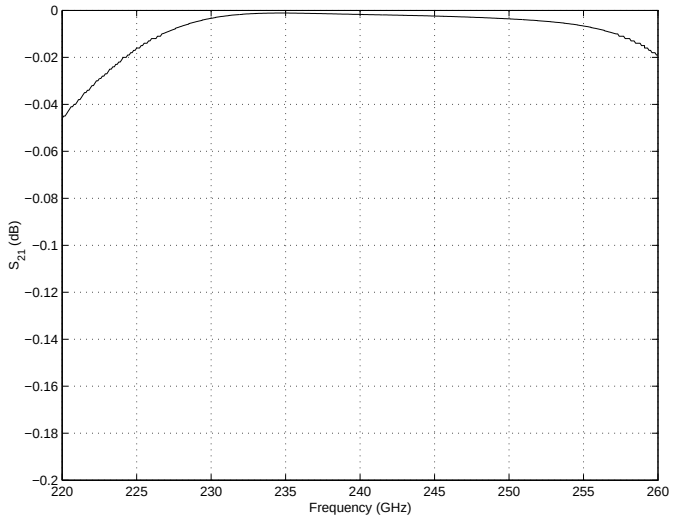

Figure 4.29: Plot of S_{21} for the complete 80/240 GHz frequency tripler output circuit (simulated).

4.5.3 Harmonic Balance Simulations

The final step in the design procedure involved computing the embedding impedances, $Z_i(f)$ and $Z_o(f)$, synthesized by the input and output networks respectively. These impedances were presented at port-1 of Figure-4.11 and harmonic balance simulations were performed to estimate the expected output power of the frequency tripler as a function of frequency. An input pump power of 50 mW was used in these calculations. Figure-4.30 shows the result of this frequency swept one-tone harmonic balance computations.

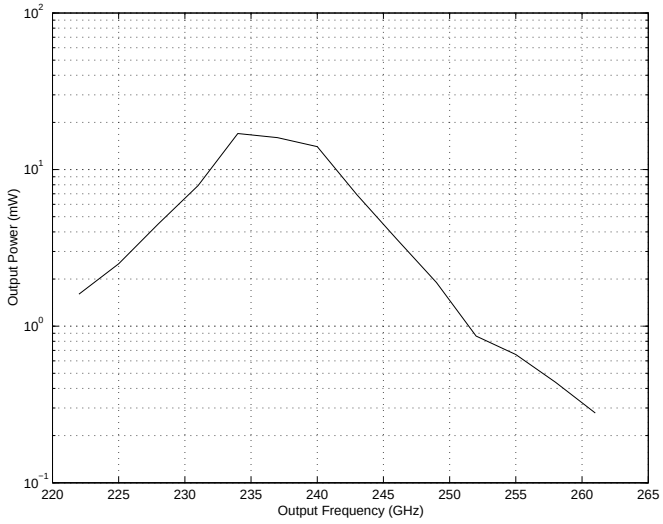

Figure 4.30: Calculated output power of the 80/240 GHz frequency tripler as a function of output frequency.

To estimate the effect of mutual loading between the input and output circuits another set of harmonic balance simulations were performed with $Z_i(3f_0)$ and $Z_o(f_0)$ set as open circuits across the entire frequency band of operation (instead of using the actual synthesized values, which were used to calculate the results shown in Figure-4.30). The resulting data are presented

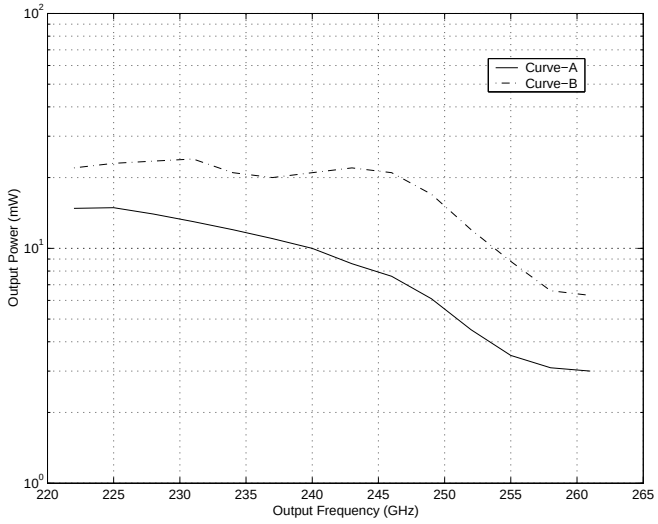

Figure 4.31: Calculated output power of the 80/240 GHz frequency tripler with the mutual loading effects between the input and output circuits ignored (curve-A). Curve-B shows the calculated output power with nearly ideal embedding impedances.

as curve-A in Figure-4.31. Comparison of the data in Figure-4.30 and curve-A of Figure-4.31 reveals that significant degradation in performance away from the center of the frequency band of operation due to the mutual loading of the input and output networks.

The reactance synthesized by the reactance tuning network in the output circuit was observed to be somewhat low. Curve-B in Figure-4.31 shows the expected output power if this deficit were to be made up for by some means.

4.6 Fabrication and Assembly

The planar input and output quartz circuits were fabricated on a 1 mil thick fused-quartz substrate using a photolithographic process. The mask was fab-

ricated on a 3 inch × 3 inch × 0.060 inch chromium soda-lime substrate and was right reading, chromium down, dark field type. The mechanical drawings of the mask used in the process are provided in Appendix-B. As shown in these drawings, both the input and output embedding circuits were included on the same mask. The procedure for the photolithographic fabrication of the circuits is provided in Appendix-C.

The metallic housing for the frequency tripler circuits was machined as a three-piece split block. The mechanical drawings of the split block pieces and their assembly are provided in Appendix-D.

A description of the procedure to house the input and output quartz circuits and attach them to the planar diode chip and the subsequent assembly of the frequency tripler block is provided in Appendix-E.

The evaluation of the completed frequency doubler is described in the following section.

4.7 Evaluation

The evaluation of the 80/240 GHz frequency tripler was carried out by driving it with a frequency tunable Gunn diode oscillator and measuring the generated output power using an appropriate power sensor and meter. The details of the arrangement are illustrated in Figure-4.32 and explained below.

The precision attenuator attached to the Gunn diode oscillator output was used as a power leveling device and was adjusted as required to avoid saturating the WM782W harmonic mixer while making frequency measurements using the spectrum analyzer. For this, the short placed on port “A” of the waveguide switch was used to reflect the incident power and frequency

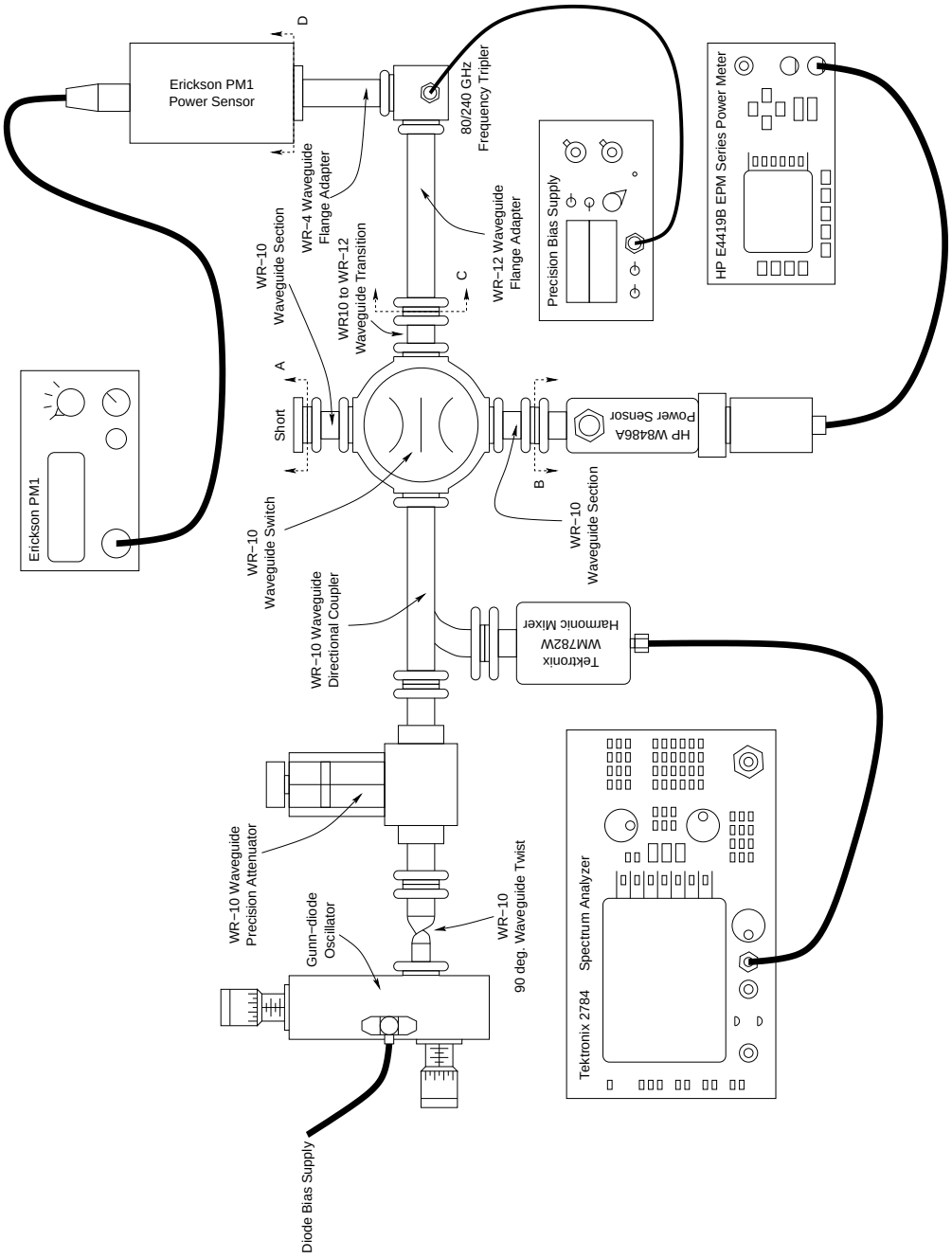

Figure 4.32: Experimental setup for evaluation of the 80/240 GHz frequency tripler.

measurements were made by the spectrum analyzer connected to the coupled port on the directional coupler through the harmonic mixer. A nominal setting of 10–15 dB was used on the precision attenuator while making frequency measurements so as to reduce the power coupled back into the Gunn diode oscillator. The HP W8486A power meter sensor attached to port "B" of the waveguide switch was used to measure the input power level to the frequency tripler, which was itself connected to port "C" of the waveguide switch. The output of the frequency tripler, appearing at section identified as "D" in the figure, was detected using an Erickson model PM1 power sensor.

The input of the frequency tripler was referenced to port "C" while its output was referenced to "D". The input WR-12 flange adapter and the output WR-4 flange adapter were considered integral to the frequency tripler for the purpose of measuring the input and output power levels and computing its flange to flange efficiency. The frequency tripler was biased using a precision bias supply and the bias current and voltage levels were monitored.

Prior to commencing each measurement, the precision attenuator was set to maximum attenuation and the waveguide switch was set to connect port "A" to the Gunn source. The frequency of the Gunn diode oscillator was then set by observing the oscillation frequency on the spectrum analyzer. The attenuation setting on the precision attenuator was lowered to raise the signal level on the spectrum analyzer, if needed, taking care not to exceed the power rating of the HP W8486A power sensor. Subsequently, the waveguide switch was set to connect the Gunn source to port "B" and precision attenuator setting was returned to zero. The reading on the HP E4419B power meter was recorded. The bias voltage to the frequency tripler was set to -10 V and the waveguide switch was set to connect the frequency tripler input (port

"C") to the Gunn source. The bias was then adjusted to maximize the output power detected by the Erickson PM1 power sensor connected at "D" and measured by the power meter. The measured output power as well as the corresponding bias voltage were recorded.

The measured performance of the 80/240 GHz frequency tripler, constructed using a diode chip with 6 μm diameter anodes, is presented in Figure-4.33. The input power levels are also shown. The 6 μm anode size was chosen over the nominal 7 μm anode size called for by the design because the measured zero bias junction capacitance of the diodes with 7 μm diameter anodes was about 90 fF, much more than the expected 54 fF per anode. The zero bias junction capacitance of the diodes with 6 μm diameter anodes was measured to be 60 fF. (This was more than than the calculated value of 47 fF for this anode size, but closer to 54 fF/anode for which the input and output circuits were designed.) The reverse breakdown voltage of the Schottky contacts was measured to be in the 8–9 V range. The DC bias bypass capacitor had a capacitance of about 1400 fF, fairly close to the calculated value of 1500 fF.

Measurements were made both in the varactor mode (with the diodes reverse biased as usual) of operation and in the varistor mode (with the diodes forward biased) of operation. For output frequencies below 228 GHz, the output power in the varistor mode of operation exceeded that in the varactor mode of operation and vice versa.

The lower than expected operational efficiency of the frequency tripler was attributed to the parasitics of the three way junction between the input and output quartz circuits and the diode chip. The amount of silver epoxy

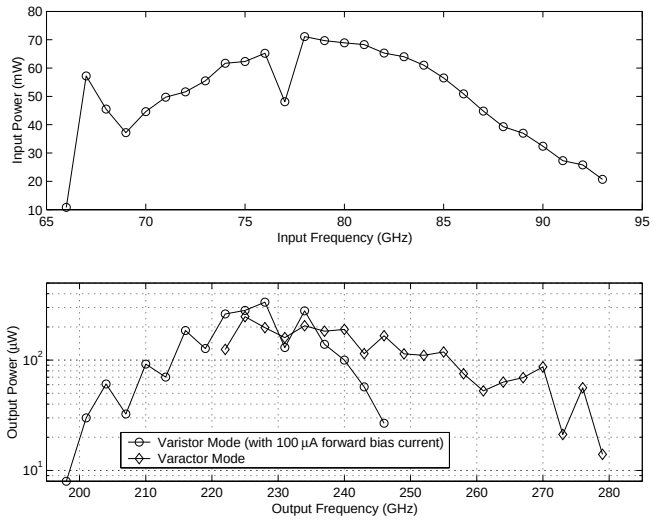

Figure 4.33: Measured performance of the 80/240 GHz frequency tripler, built using a diode chip having 6 μm diameter anodes.

required for implementing the "3-D" junction was large enough to result in significant capacitive parasitic with the walls of the metal housing. This resulted in a loss of power for both the fundamental pump signal as well as the generated third harmonic. Furthermore, the input circuit was designed to appear as an open circuit at 240 GHz while the output circuit was designed to do so at 80 GHz in order to prevent the circuits from loading each other as described in Section-4.2. Due to the tolerances in the metal block and the realized junction geometry, this aspect of the design was also in question– causing the operating impedance levels to depart from the desired optimum and negatively impact both the conversion efficiency at the diode level as well as the coupling efficiency of the waveguide probes used in the linear input and output coupling circuits.

4.8 Redesign of the 80/240 GHz Frequency Tripler

To alleviate the problems encountered with the previous iteration of the frequency tripler, it was decided to fabricate the input and output linear embedding circuits on a single quartz substrate. Besides allowing tighter control over the interaction between the two circuits this allowed a simplification in the structure of the metal housing. The metal housing was designed to have the quartz circuit coplanar with the diode chip, thus permitting a simpler two-piece split block construction as shown in Figure-4.34.

4.8.1 Design of the Linear Embedding Circuit

The layout of the quartz circuit implementing the combined input and output linear embedding networks is illustrated in Figure-4.35. The input and output waveguide to microstrip transitions were carried forward from the previous design and remained unchanged. Ports 1, 2 and 3 were defined as indicated and the circuit optimized to synthesize the desired impedance and transmission characteristics on these ports.

Figure-4.36 shows the circuit dimensions that were optimized to complete the design. The radius, d_{28}, of the radial line stub in the input circuit was optimized to prevent the third harmonic power from propagating towards the input waveguide. Figure-4.37 shows the achieved isolation. The distance of the radial line stub from the junction of the input network with the output network (port-2), marked as d_{21}, was optimized to synthesize the input embedding impedance required to be presented to the diode chip (as described

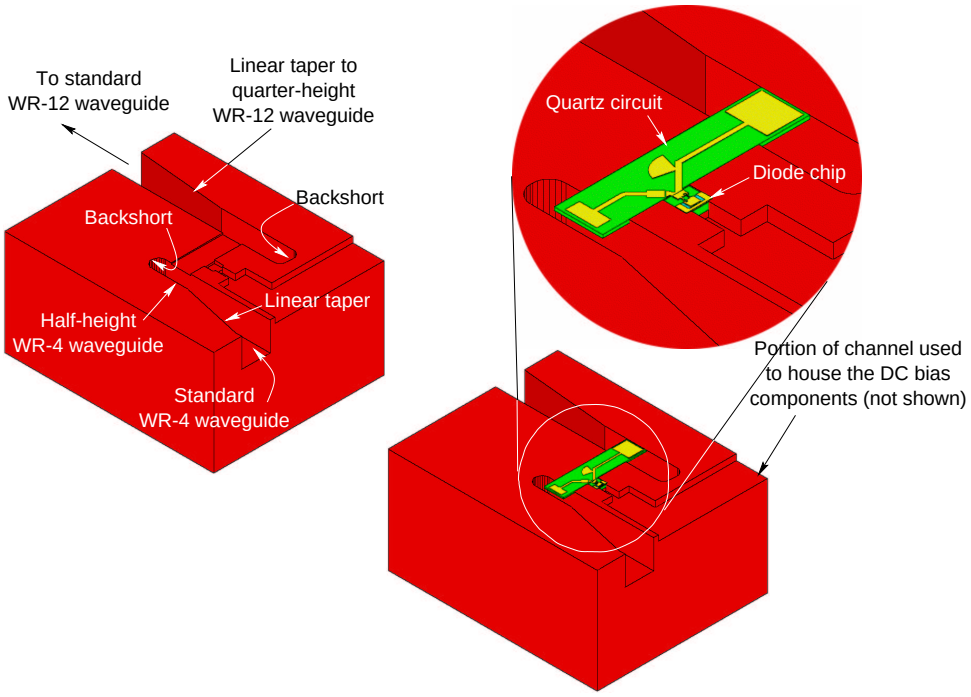

Figure 4.34: The modified 80/240 GHz frequency tripler. Figure shows a cut-away view of the split block mount revealing the location of the planar quartz circuit and the placement of the diode chip alongside it. The DC bias components and bond wires are omitted.

in Section-4.5). The overall length of the input microstrip line, d_{20}, was optimized to make the input circuit present an open circuit at the output frequency of 240 GHz at port-2 (junction of the input circuit with the diode chip and the output circuit).

As was the case with the input circuit, the output circuit was also optimized to synthesize the desired output embedding impedance required to be presented to the diode chip (as described in Section-4.5), as well as to make the output circuit appear as an open circuit at the input frequency of 80 GHz at port-2 (junction of the output circuit with the diode chip and the input

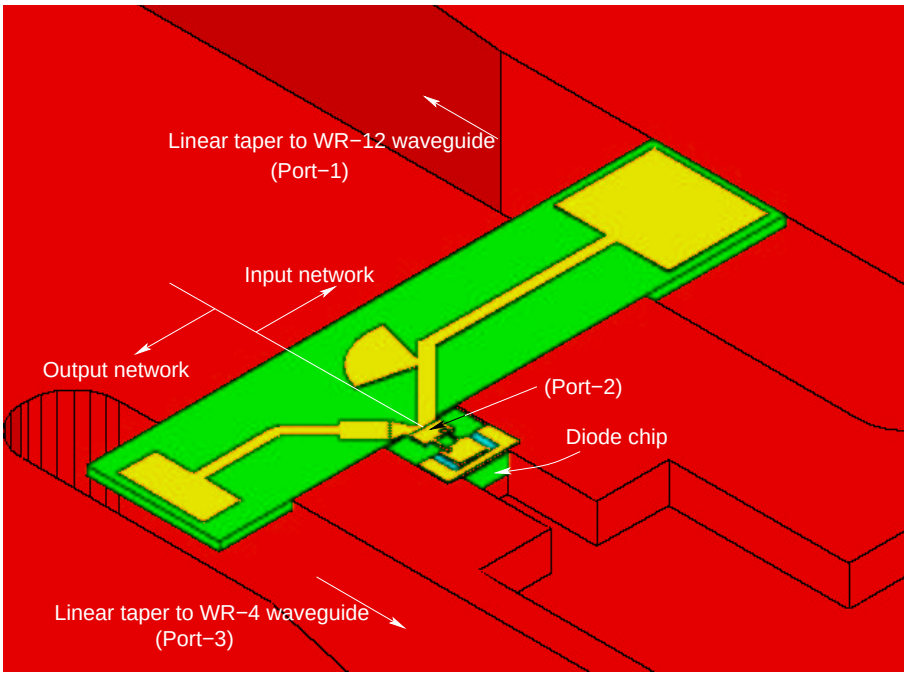

Figure 4.35: Layout of the input and output embedding circuits, integrated onto a single quartz substrate. Also illustrated is the placement of the quartz circuit relative to important features on the metal block as well as the diode chip. Only bottom half of the mount that seats the circuits is shown.

circuit). Dimensions d_{22}, d_{23}, d_{24}, d_{25} as well as the gap of the capacitive coupling (identified in Figure-4.36) were optimized to achieve this goal.

4.8.2 Fabrication and Assembly

The planar quartz circuits were fabricated on a 1 mil thick fused-quartz substrate using a photolithographic process. The mask was fabricated on a 3 inch $\times$ 3 inch $\times$ 0.060 inch chromium soda-lime substrate and was right reading, chromium down, dark field type. The mechanical drawings of the mask used in the process are provided in Appendix-B. As shown in these

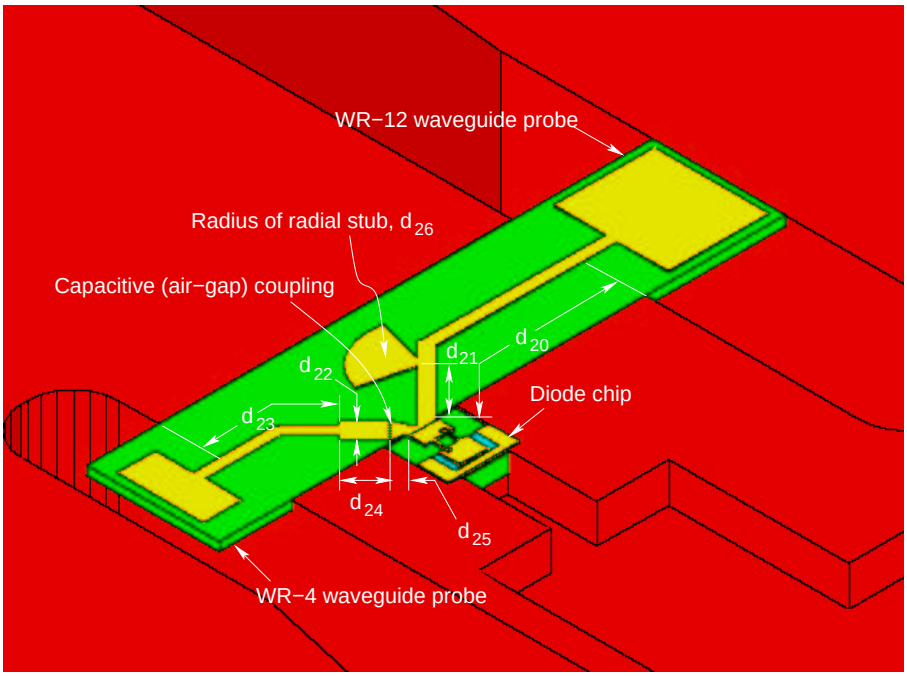

Figure 4.36: Design of the input and output embedding circuits. All the dimensions that were optimized are marked. The design of the 50 Ω microstrip to waveguide transition for both the input and output was carried forward from the previous block. Consequently, dimensions corresponding to those transitions did not need to be optimized. Only bottom half of the mount that seats the circuits is shown.

drawings, both the input and output embedding circuits were included on the same mask. The procedure for the photolithographic fabrication of the circuits is provided in Appendix-C.

The metallic housing for the frequency tripler circuits was machined as a two-piece split block. The mechanical drawings of the split block pieces and their assembly are provided in Appendix-D.

A description of the procedure to house the quartz circuit and attach it to the planar diode chip and the subsequent assembly of the frequency tripler block is provided in Appendix-E.

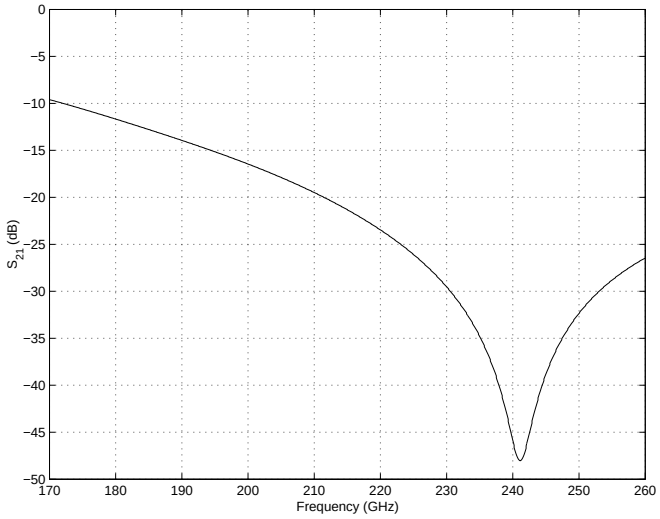

Figure 4.37: Plot of S_{21} for the modified 80/240 GHz frequency tripler quartz circuit showing the isolation provided by the radial stub in the input circuit to the third harmonic signals (simulated).

The evaluation of the completed frequency tripler is described in the following sub-section.

4.8.3 Evaluation

The evaluation of the modified 80/240 GHz frequency tripler was carried out using the same experimental setup that was used earlier (as described in Section-4.7) to test the previous version of the frequency tripler. Additionally, a higher frequency Gunn diode oscillator and a lower frequency klystron oscillator were used to extend the upper and lower limits of the input test frequency range. The rest of the measurement procedure remained the same as before.

The measured performance of the 80/240 GHz frequency tripler, constructed using a diode chip with 6 μm diameter anodes, is presented in

Figure-4.38. The input power levels are also shown. As done earlier, the 6 μm anode size was chosen over the nominal 7 μm anode size called for by the design because the measured zero bias junction capacitance of the diodes with 7 μm diameter anodes was about 90 fF, much more than the expected 54 fF per anode. The zero bias junction capacitance of the diodes with 6 μm diameter anodes was measured to be 60 fF. (This was more than than the calculated value of 47 fF for this anode size, but closer to 54 fF/anode for which the input and output circuits were designed.) The reverse breakdown voltage of the Schottky contacts was measured to be in the 8–9 V range.

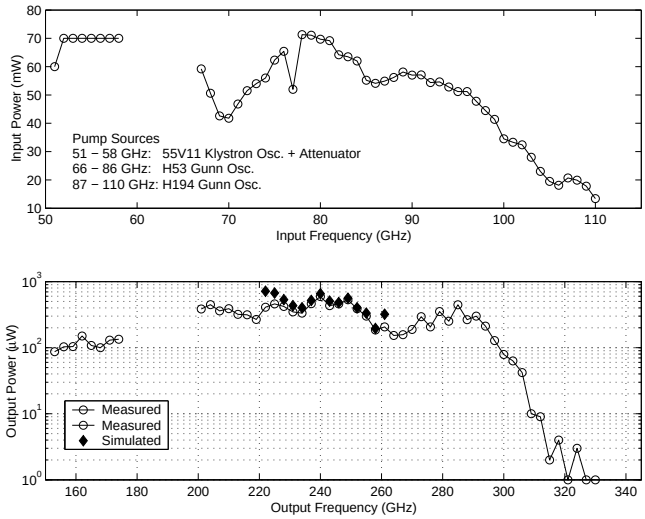

Figure 4.38: Performance of the modified 80/240 GHz frequency tripler built using a diode chip having 6 μm diameter anodes, with the DC bias bypass capacitor shorted to the ground pad with silver epoxy.

The DC bias bypass capacitors exhibited a low reverse breakdown voltage of around 6–8 V, rendering the optimal operation of the frequency tripler in varactor mode impossible. For the purpose of this evaluation, the frequency tripler was modified by shorting out the bias bypass capacitor to the ground

pad using silver epoxy. This allowed for the operation of the frequency tripler with the offending circuit element bypassed and under the conditions of zero applied DC bias voltage on the Schottky diodes. To allow for a comparison between the measured and theoretical performance under these conditions, swept harmonic balance simulations were performed (with the DC bias voltage set to zero) in MDS to estimate the predicted output power of the frequency tripler. Calculated output power levels obtained as a result of these simulations are shown plotted along with the measured data in Figure-4.38.

In order to identify a diode chip with a good DC bias bypass capacitor, all the diode chips with 6 μm diameter anodes were examined but showed a low reverse breakdown of the DC bias bypass capacitor subsequent to assembly into the block with silver epoxy and curing. Close observation under the scanning electron microscope did not reveal any obvious cause for this deterioration. Defects in the n^- layer are thought to be the cause of the low reverse breakdown voltage. The reverse breakdown voltages of the RF diodes themselves were within a volt of their theoretically calculated values. This problem could be resolved by replacing the present DC bias structure with a conventional MIM capacitor. The lossy nature of the dielectric should not induce any significant series resistance due to the large cross-sectional area of the structure.

4.9 Conclusion

Notwithstanding the inability to measure its optimum varactor-mode performance, the good agreement between the measured and theoretical performance of the 80/240 GHz frequency tripler under zero applied DC bias (as

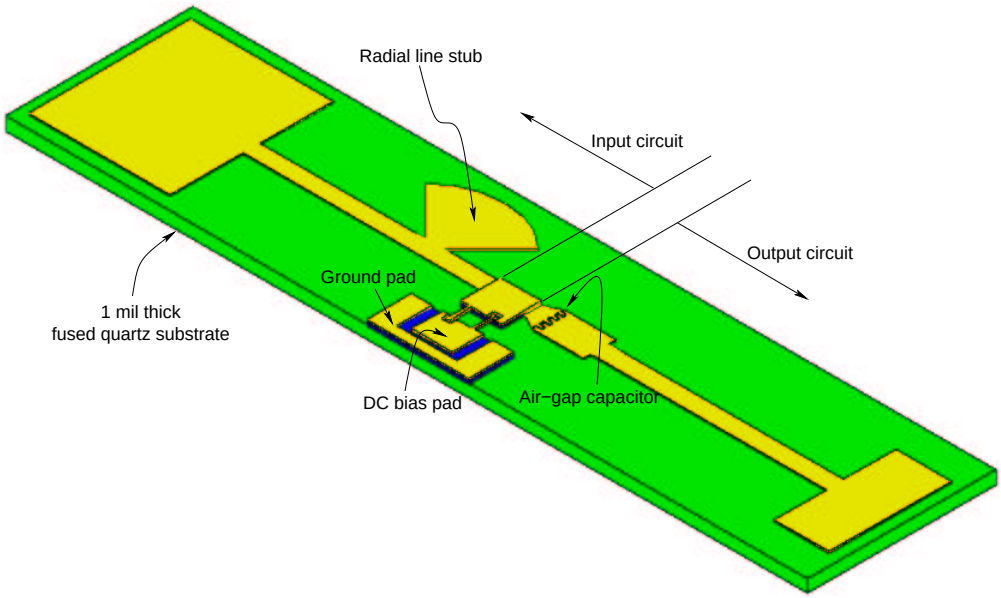

Figure 4.39: Layout of the 80/240 GHz frequency tripler as a MMIC chip. The embedding circuits may be fabricated integrally as shown on the extended GaAs-membrane-on-quartz substrate after the removal of GaAs from appropriate regions.

illustrated by Figure-4.38) validates the use of GaAs-membrane-on-quartz substrates for the design of monolithic frequency multipliers in the 100–300 GHz frequency range. Figure-4.39 shows a possible layout of the frequency tripler as a MMIC chip, based on the 80/240 GHz frequency multiplier investigated in this chapter.

Chapter 5

Noise Analysis

Fluctuations in signal amplitude (termed "AM noise") and phase (termed "PM noise") of a local oscillator signal have a crucial bearing on the sensitivity of a frequency converting millimeter- and submillimeter-wave receiver. AM noise in a LO signal degrades the noise factor of a receiver, particularly if an unbalanced mixer is employed for frequency down-conversion. The PM noise in the LO signal is almost always transferred directly into the signal, as a result of frequency conversion in the mixer, making it detrimental to the performance of receivers where the phase is important. For instance in interferometric receivers, phase noise can contribute to a degradation in the coherence amongst signals in various channels of the receiver. This chapter

focuses on the study of frequency multipliers from the point of view of the noise in the generated LO signal.

5.1 Introduction

With rapid advances in low-noise-temperature receiver technology, the noise in the LO signal is poised to become an increasingly important factor limiting the actual sensitivity of millimeter- and submillimeter-wave receivers. With frequency multipliers being an important building block of any practical LO system, their noise characteristics have an important bearing on the noise performance of the receiver. This chapter focuses on the analysis of their noise transmission characteristics.

The first part of this chapter presents a rudimentary analysis based on an extension of periodic steady-state relationships to the case of slowly varying amplitude and phase of the input signal. Such an analysis adequately predicts the noise properties of a typical frequency multiplier near the pump frequency but is inadequate for describing the noise characteristics at a frequency offset far removed from the pump frequency, where the periodic steady-state relationships assumed in the analysis no longer accurately describe the frequency multiplier operation. The criteria delimiting what can be considered small frequency offset and what has to be regarded as a large offset depends primarily on the type and order of the frequency multiplier, and on the amount of acceptable error. The noise properties far away from the pump frequency are important characteristics nevertheless, particularly in cases where the un-filtered output of a frequency multiplier is used to pump a frequency converter having large IF bandwidth (often the case in many millimeter- and

submillimeter-wave receivers), and their accurate prediction is investigated in the later portion of this chapter.

An analytical technique based on a linear analysis of noise conversion could be employed for this purpose. However, for the purpose of this study, multi-tone harmonic balance simulations were carried out in Hewlett Packard's Microwave & Design System (MDS) [145] to essentially yield the same information and help gain an understanding of the noise propagation process. The second part of this chapter presents the results of this analysis, characterizing the conversion of the input sideband noise, and describing the noise characteristics of a frequency multiplier at large offsets from the pump frequency.

5.2 Static Analysis of Noise Transmission

The response of a frequency multiplier to a change in the amplitude or phase (or frequency[1]) of the input signal settles after a duration that depends on the bandwidth of the circuit. If the amplitude and phase (or frequency) fluctuations of the input signal driving a non-linear circuit are sufficiently slow, then each signal in the circuit can be considered as a superposition of all the harmonic components, whose phase and amplitude follow the changes in the input signal. Since the relationships between the amplitude and phase of slowly varying components are the same as in the periodic steady-state, an

[1]The fluctuations in the phase, ϕ, of a signal may be represented in terms of the fluctuations in its frequency, ω, due to the relation, $\omega = \frac{d\phi}{dt}$. Thus any analysis describing either the phase noise performance or the frequency noise performance, completely describes the other.

analysis based on the "slowly varying" input signal as presented below, may be termed as "static" analysis. The goal of such an analysis is to relate the amplitude and phase noise power spectra of a frequency multiplier output to the amplitude and phase noise power spectra of its input signal. This relationship is expressed in terms of a noise transmission matrix [158]. The derivation of the noise transmission matrix and its application in computing the the output noise densities are presented below.

5.2.1 Time Domain Description

The analysis presented in this sub-section relates the amplitude and phase fluctuations in the output of the frequency multiplier to those present in the input pump signal. These results are used to derive the noise transmission matrix in the following sub-section.

Let the input pump signal to a $\times n$ frequency multiplier be given by

$$e(t) = E\ cos(2\pi ft + \phi_e) \tag{5.1}$$

where f is the frequency of the input pump signal, having an amplitude E[2] and an initial phase ϕ_e. The output signal of the frequency multiplier may then be written as

$$v(t) = V(E, f)\ cos\ \varphi_v \tag{5.2}$$

where

$$\varphi_v = 2\pi nft + n\phi_e + \phi_v(E, f) \tag{5.3}$$

As explicitly stated by the notation, the amplitude of the output signal as well as its phase depend upon the amplitude and frequency of the input

[2]Note that this usage of the symbol E departs from the usual notation used elsewhere in this dissertation, where E denotes the electric field.

signal. The argument of the cosine function, φ_v, represents the phase of the output signal. Its component $n\phi_e$ represents the phase change in the output signal corresponding to a change in the initial phase of the input signal, whereas $\phi_v(E, f)$ is a non-linear phase term representing the additional phase (dependent on the input signal) engendered in the frequency multiplier.

If $E_o = \langle E \rangle$ is defined as the average value of the input signal amplitude, then the instantaneous amplitude of the input signal may be written as

$$E(t) = E_o(1 + \Delta a_e(t)) \tag{5.4}$$

where $\Delta a_e(t)$ represents the amplitude noise in the input signal. Similarly the instantaneous input frequency may be represented in terms of the average input frequency, f_o, and the slowly varying phase (frequency) of the input signal represented by $\Delta f_e(t)$ as

$$f(t) = f_o + \Delta f_e(t) \tag{5.5}$$

The instantaneous amplitude, $V(t)$, and phase, $\varphi_v(t)$, of the output signal may then be written as

$$V(t) = V(E_o + E_o \Delta a_e(t), f_o + \Delta f_e(t)) \tag{5.6}$$

$$\varphi_v(t) = \left[2\pi n \int_0^t (f_o + \Delta f_e(t))dt\right] + n\phi_e + \phi_v(E_o + E_o \Delta a_e(t), f_o + \Delta f_e(t)) \tag{5.7}$$

Again, defining $V_o = \langle V(E_o, f_o) \rangle$ as the average value of the output signal amplitude, the instantaneous output amplitude may be defined in terms of the output amplitude noise, $\Delta a_v(t)$, as follows

$$V(t) = V_o(1 + \Delta a_v(t)) \tag{5.8}$$

The amplitude noise of the output signal may therefore be expressed in terms of the input amplitude and phase noise by re-writing the relations expressed in Equations-5.6 and 5.8 as a Taylor's series about (E_o, f_o) as follows

$$V_o \Delta a_v(t) = \frac{\partial V}{\partial E}\bigg|_{E_o} E_o \Delta a_e(t) + \frac{\partial V}{\partial f}\bigg|_{f_o} \Delta f_e(t) \tag{5.9}$$

which can be re-arranged to yield

$$\Delta a_v(t) = \frac{\partial V}{\partial E}\bigg|_{E_o} \frac{E_o}{V_o} \Delta a_e(t) + \frac{\partial V}{\partial f}\bigg|_{f_o} \frac{1}{V_o} \Delta f_e(t) \tag{5.10}$$

Similarly, the phase noise in the output signal of Equation-5.2 may be expressed in terms of the input amplitude and phase noise as

$$\Delta \varphi_v(t) = 2\pi n \int_0^t \Delta f_e(t) dt + \frac{\partial \phi_v}{\partial E}\bigg|_{E_o} E_o \Delta a_e(t) + \frac{\partial \phi_v}{\partial f}\bigg|_{f_o} \Delta f_e(t) \tag{5.11}$$

5.2.2 Noise Transmission Matrix

The time domain equations relating the amplitude and phase noise at the frequency multiplier output with the amplitude and phase noise of the input pump signal, obtained above, may be Fourier transformed and the results used to extract the noise transmission matrix.

Noting that relation between the quantity $\Delta f_e(t)$ that was used to represent the input phase noise and the actual input phase noise $\Delta \phi_e(t)$ is

$$\Delta f_e(t) = \frac{1}{2\pi} \frac{d}{dt} \Delta \phi_e(t) \tag{5.12}$$

Equation-5.10 may be re-written as

$$\Delta a_v(t) = \frac{\partial V}{\partial E}\bigg|_{E_o} \frac{E_o}{V_o} \Delta a_e(t) + \frac{\partial V}{\partial f}\bigg|_{f_o} \frac{1}{V_o} \left(\frac{1}{2\pi} \frac{d}{dt} \Delta \phi_e(t) \right) \tag{5.13}$$

Let $\Delta a_v(t) \leftrightarrow \delta A_v(f)$, $\Delta a_e(t) \leftrightarrow \delta A_e(f)$, and $\Delta \phi_e(t) \leftrightarrow \delta \Phi_e(f)$ define the Fourier transform pairs. Noting that differentiation in time domain corresponds to multiplication by the factor $(j2\pi f)$ in the frequency domain, we can transform Equation-5.13 to get

$$\delta A_v(f) = \frac{\partial V}{\partial E}\bigg|_{E_o} \frac{E_o}{V_o}\delta A_e(f) + \frac{\partial V}{\partial f}\bigg|_{f_o} \frac{j2\pi f}{2\pi V_o}\delta \Phi_e(f) \tag{5.14}$$

which can be simplified to yield the spectrum of the amplitude noise component at the multiplier output

$$\delta A_v(f) = \frac{jf}{V_o}\frac{\partial V}{\partial f}\bigg|_{f_o} \delta \Phi_e(f) + \frac{\partial V}{\partial E}\bigg|_{E_o} \frac{E_o}{V_o}\delta A_e(f) \tag{5.15}$$

Similarly Equations-5.11 and 5.12 together yield

$$\Delta \varphi_v(t) = 2\pi n \int_0^t \left(\frac{1}{2\pi}\frac{d}{dt}\Delta \phi_e(t)\right)dt + \frac{\partial \phi_v}{\partial E}\bigg|_{E_o} E_o \Delta a_e(t) + \frac{\partial \phi_v}{\partial f}\bigg|_{f_o} \left(\frac{1}{2\pi}\frac{d}{dt}\Delta \phi_e(t)\right) \tag{5.16}$$

After defining another Fourier transform pair $\Delta \varphi_v(t) \leftrightarrow \Delta \Phi_v(f)$, this gives

$$\delta \Phi_v(f) = n\delta \Phi_e(f) + \frac{\partial \phi_v}{\partial E}\bigg|_{E_o} E_o \delta A_e(f) + \frac{\partial \phi_v}{\partial f}\bigg|_{f_o} \frac{j2\pi f}{2\pi}\delta \Phi_e(f) \tag{5.17}$$

Simplifying further, we get the spectrum of the phase noise component in the multiplier output

$$\delta \Phi_v(f) = n\delta \Phi_e(f) + jf\frac{\partial \phi_v}{\partial f}\bigg|_{f_o} \delta \Phi_e(f) + \frac{\partial \phi_v}{\partial E}\bigg|_{E_o} E_o \delta A_e(f) \tag{5.18}$$

Equations-5.15 and 5.18 may be combined using matrix notation to yield

$$\begin{bmatrix} \delta \Phi_v(f) \\ \delta A_v(f) \end{bmatrix} = \begin{bmatrix} n + jf\frac{\partial \phi_v}{\partial f} & \frac{\partial \phi_v}{\partial E}E_o \\ j\frac{f}{V_o}\frac{\partial V}{\partial f} & \frac{\partial V}{\partial E}\frac{E_o}{V_o} \end{bmatrix} \begin{bmatrix} \delta \Phi_e(f) \\ \delta A_e(f) \end{bmatrix} \tag{5.19}$$

All the partial derivatives are understood to have been evaluated at (E_o, f_o) as was the case in Equations-5.15 and 5.18 earlier. Furthermore the frequency term, f, refers to the offset from the pump frequency, since the Fourier series expansion was carried out about that operating frequency, f_o.

Thus the output amplitude and phase noise of a multiplier is related to the amplitude and phase noise of the input signal through the noise transmission matrix

$$\begin{bmatrix} \delta\Phi_v(f) \\ \delta A_v(f) \end{bmatrix} = \begin{bmatrix} T_{\phi\phi}(f) & T_{\phi a} \\ T_{a\phi}(f) & T_{aa} \end{bmatrix} \begin{bmatrix} \delta\Phi_e(f) \\ \delta A_e(f) \end{bmatrix} \tag{5.20}$$

where the individual elements of the noise transmission matrix are defined by

$$\mathbf{T}(f) = \begin{bmatrix} T_{\phi\phi}(f) & T_{\phi a} \\ T_{a\phi}(f) & T_{aa} \end{bmatrix} = \begin{bmatrix} n + jf\frac{\partial\phi_v}{\partial f} & \frac{\partial\phi_v}{\partial E}E_o \\ j\frac{f}{V_o}\frac{\partial V}{\partial f} & \frac{\partial V}{\partial E}\frac{E_o}{V_o} \end{bmatrix} \tag{5.21}$$

For small offsets from the operating frequency, $f \to 0$, $\mathbf{T}(f)$ can be simplified to yield

$$\mathbf{T} = \begin{bmatrix} n & \frac{\partial\phi_v}{\partial E}E_o \\ 0 & \frac{\partial V}{\partial E}\frac{E_o}{V_o} \end{bmatrix} \tag{5.22}$$

5.2.3 Output Noise Densities

The noise transmission matrix allows for the calculation of output amplitude and phase noise power spectra from the knowledge of the amplitude and phase noise power spectra of the input pump signal.

Let $\mathbf{S_e}(f)$ represent the input noise power spectrum

$$\mathbf{S_e}(f) = \begin{bmatrix} S_e^{\phi\phi}(f) & S_e^{\phi a}(f) \\ S_e^{a\phi}(f) & S_e^{aa}(f) \end{bmatrix} \tag{5.23}$$

where $S_e^{\phi\phi}(f)$ is the input phase noise power spectrum, $S_e^{aa}(f)$ is the input amplitude noise power spectrum. $S_e^{\phi a}(f)$ and $S_e^{a\phi}(f)$ represent the AM–PM cross-correlation terms. Similarly, let $\mathbf{S_v}(f)$ represent the output noise power spectrum

$$\mathbf{S_v}(f) = \begin{bmatrix} S_v^{\phi\phi}(f) & S_v^{\phi a}(f) \\ S_v^{a\phi}(f) & S_v^{aa}(f) \end{bmatrix} \tag{5.24}$$

The input and output noise power spectra are related through the noise transmission matrix, $\mathbf{T}(f)$, as follows

$$\mathbf{S_v}(f) = \mathbf{T}(f)\mathbf{S_e}(f)\mathbf{T}(f)^{+} \tag{5.25}$$

where the symbol $^{+}$ represents a complex conjugate transpose. Thus the output phase noise power spectrum may be calculated from

$$S_v^{\phi\phi} = n^2 S_e^{\phi\phi} + \left(\frac{\partial \phi_v}{\partial E} E_o\right)^2 S_e^{aa} + 2n\frac{\partial \phi_v}{\partial E} E_o Re\{S_e^{\phi a}\} \tag{5.26}$$

while the output amplitude noise power spectrum may be computed from

$$S_v^{aa} = \left(\frac{\partial V}{\partial E}\frac{E_o}{V_o}\right)^2 S_e^{aa} \tag{5.27}$$

The AM–PM cross-correlation terms in the output signal may be computed in a similar fashion using Equation-5.25.

The well known results for an ideal lossless frequency multiplier are implicit in these relations. For an ideal lossless frequency multiplier without gain compression (i.e. with a small signal gain $\partial V/\partial E$ equal to V_o/E_o resulting in $T_{aa} = 1$), and without noise conversion from AM to PM or vice versa, the noise transmission matrix reduces to

$$\mathbf{T} = \begin{bmatrix} n & 0 \\ 0 & 1 \end{bmatrix} \tag{5.28}$$

Thus in the case of an ideal frequency multiplier, the phase noise power spectral density at the output is n^2 higher than the input phase noise power spectral density (second and third terms in Equation-5.26 become zero). Similarly, the squared term in Equation-5.27 becomes unity, implying that the output amplitude noise power spectral density is identical to the input amplitude noise power spectral density for the case of an ideal frequency multiplier.

For almost all the other cases, an evaluation of the elements of the noise transmission matrix of Equation-5.21 requires knowledge of the actual frequency multiplier circuit as well as the input frequency, f_o, and drive power level, E_o. Swept one-tone harmonic balance simulations may then be performed around (E_o, f_o) and used to plot the output phase, ϕ_v, and the output amplitude, V, as a function of pump frequency and amplitude to evaluate $\frac{\partial \phi_v}{\partial f}\Big|_{f_o}$, $\frac{\partial V}{\partial f}\Big|_{f_o}$, $\frac{\partial \phi_v}{\partial E}\Big|_{E_o}$, and $\frac{\partial V}{\partial E}\Big|_{E_o}$. These values can then be used to compute the noise transmission matrix using Equation-5.21.

5.3 Analysis of Sideband Noise Conversion

As mentioned earlier, the static analysis presented in the preceding section adequately predicts the noise performance of a frequency multiplier near its pump frequency. It does not, however, account for its noise performance far away from the pump frequency. The sideband noise is important in receivers employing frequency converters with high intermediate frequencies.

5.3.1 Noise Analysis by Linear Frequency Converter Technique

One of the techniques to analyze the conversion of sideband noise is given in [158] and involves treating the frequency multiplier as a linear frequency mixer and employing the principles of linear frequency converters to model the output sideband noise as up-converted input signal sideband noise. This involves calculation of conversion matrices (as a function of frequency offset from the carrier) to relate the spectrum of the generated output sidebands $(\delta V_u(f), \delta V_l(f))$ to the input sideband spectrum $(\delta E_u(f), \delta E_l(f))$ as illustrated in Figure-5.1.

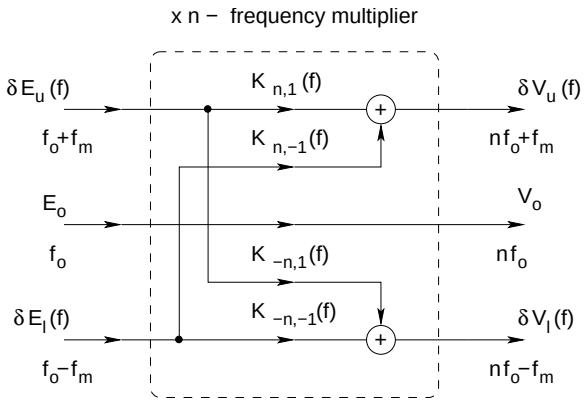

Figure 5.1: Transmission of sideband noise through a frequency multiplier, considered as a linear frequency converter.

The upper sideband noise $\delta E_u(f)$ as well as the lower sideband noise $\delta E_l(f)$ in the input signal may be calculated by modulating the input amplitude and phase noise spectra on the input carrier signal. Similarly, the output amplitude and phase noise spectra may be obtained from the knowledge of the upper and lower modulated output noise spectra, $\delta V_u(f)$ and $\delta V_l(f)$ respectively.

Of course, calculation of all the transmission coefficients, $K_{\pm n,\pm 1}(f)$, requires the knowledge of the actual frequency multiplier circuit as well as the frequency and level of the input pump signal. The coefficients could be generated via harmonic balance calculations as is generally done for mixer analysis.

In practical applications, the modulated sideband noise spectrum of the multiplier input (or pump) signal is usually known through specifications or by direct measurement whereas an estimation of the modulated output noise spectrum generally suffices. This may be achieved by two-tone harmonic balance analysis, as described below, to model the up-conversion of the input sideband noise spectrum to the the output of the frequency multiplier.

5.3.2 Noise Analysis by Two-Tone Harmonic Balance Simulations

The frequency up-conversion of the input noise sidebands in frequency multipliers was studied by using a two-tone test signal as the input in harmonic balance simulations carried out in MDS. As shown in Figure-5.2, one component of the test input was the fixed fundamental pump signal while the other was a small amplitude (about 100 dB less than the pump signal power) tone at a frequency offset of "f" from the pump frequency. Also shown alongside in the figure is the typical output power spectrum obtained from the harmonic balance simulations. Single diode based frequency doubler, tripler and quintupler were analyzed. The frequency doubler and tripler were analyzed in their usual varactor mode of operation with an input frequency of 80 GHz. The diode model used in the simulations had a zero bias junction capacitance

(C_{j0}) of 28 fF and a parasitic series resistance (R_s) of 2 Ω. Subsequently, analysis was also performed on a frequency doubler, tripler and a quintupler designed for varistor mode operation. No reverse bias was used for these simulations. The diode model used in this case was an ideal Schottky junction with zero parasitic series resistance. The zero bias junction capacitance was also set to zero to reflect the fact that Schottky diodes optimized for varistor operation are generally designed to have very little junction capacitance.

5.3.3 Simulation Strategy

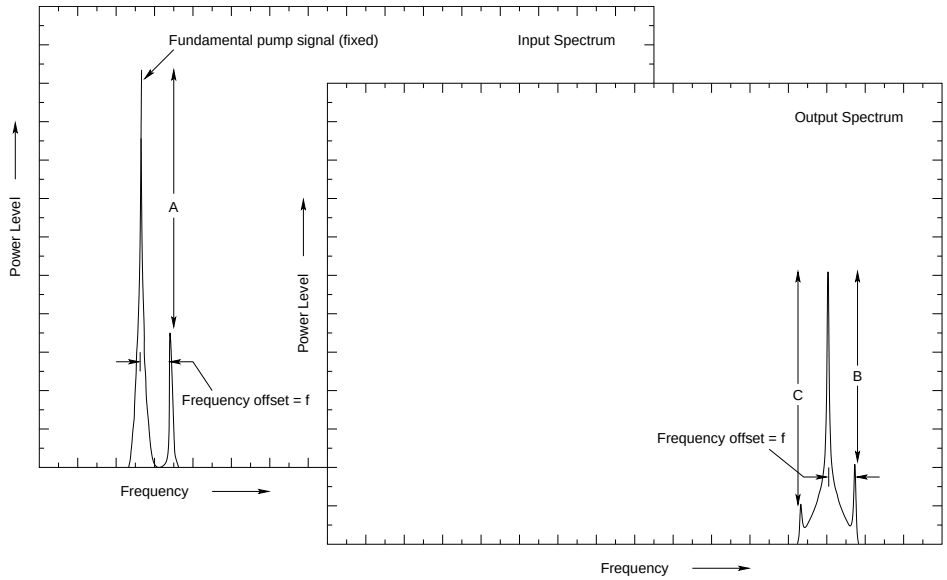

Figure 5.2: Sketches illustrate the power spectrum of the test input signal used in two-tone harmonic balance simulations (left) and the typical resulting output power spectrum (right).

The figure of merit of any LO signal may be specified by its sideband noise power expressed as a noise temperature in kelvins per milli- or micro-

watt of the available LO drive power[3]. This can be directly related to the carrier to sideband power level ratio. Therefore the carrier to sideband ratio, marked as "A" in the figure, was used to represent the quality of the pump signal to the frequency multiplier. In the presence of continuum sideband noise at the input, the power generated at any particular offset in the upper (or lower) output sideband should comprise of translated components from both upper and lower input sidebands. However, as indicated in Figure-5.2, two-tone harmonic balance simulations revealed that the power generated in the lower (or upper) output sideband by an input in the upper (or lower) sideband was much smaller (at least 7–10 dB less) than that generated in the upper (or lower) output sideband. Therefore the smaller of the two components was ignored, circumventing the issue of having to add two possibly correlated signals. The carrier-to-sideband ratio, marked as "B" in the figure, was used to represent the the quality of the LO signal generated by the frequency multiplier. The difference between the two ratios A and B was used as a measure of the signal degradation caused by the frequency multiplier. A series of harmonic balance simulations were performed to measure this degradation as a function of offset frequency.

5.3.4 Circuit Configuration

Figure-5.3 shows the configuration of a generalized $\times n$ frequency multiplier circuit used in the harmonic balance analysis. Optimum input and output embedding resistances and inductances as well as idler inductances were first

[3]This method of specifying the noise in the LO signal has the advantage that it expresses the spectral noise density as a fraction of the carrier power and makes the figure of merit independent of any attenuation that the LO signal might undergo.

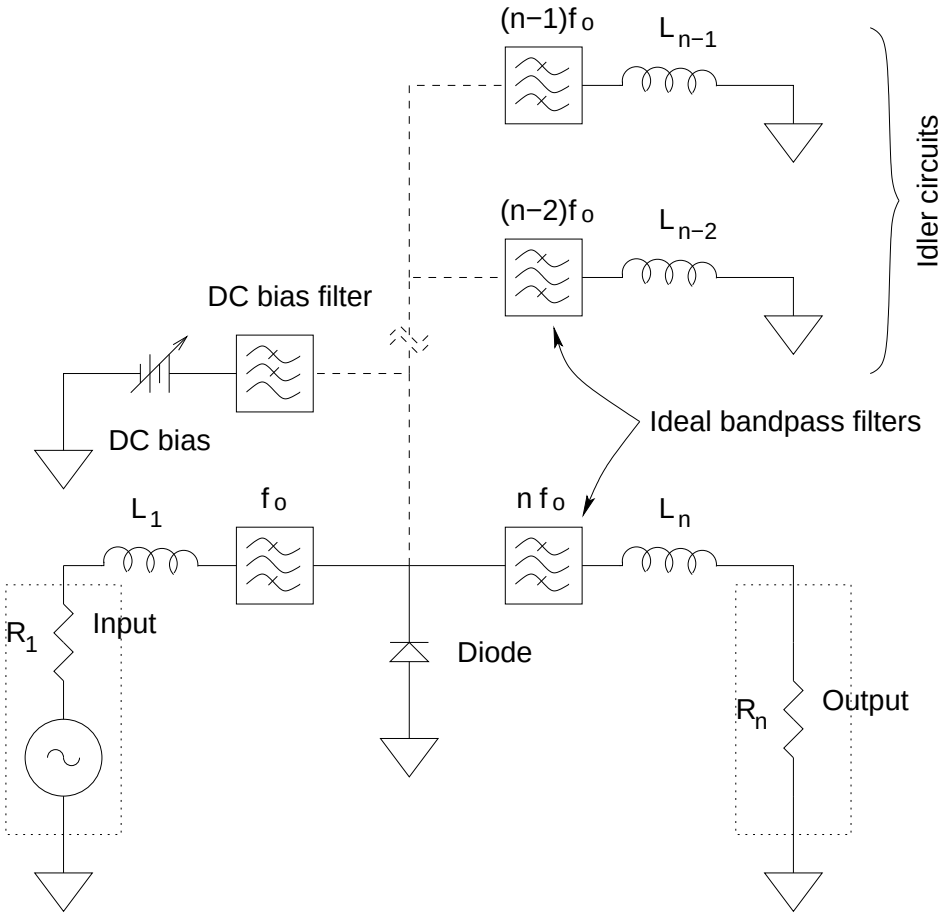

Figure 5.3: Generalized configuration of the circuit used in two-tone harmonic balance simulations to evaluate the up-conversion of amplitude-noise sidebands in $\times n$ single-diode frequency multipliers. The idler and bias circuits were used, as appropriate, for setting up various frequency multipler simulations.

computed based on single tone harmonic balance analyses for an output power of 100 μW in each case. In varistor mode operation, the optimum values for all the reactive elements turned out to be zero, making the embedding network completely resistive. The efficiencies realized in the various cases were: 80/160 GHz varactor doubler–50%, 80/160 GHz varistor doubler–20%, 80/240 GHz varactor tripler–33%, 80/240 GHz varistor tripler–7%, and

80/500 GHz varistor quintupler–1%. These compare well with the reported efficiencies of real frequency multipliers.

5.3.5 Simulation Results

Two-tone harmonic balance simulations, as described earlier, were performed on the optimized circuits and the offset frequency was swept to calculate the carrier-to-sideband noise degradation as a function of frequency. The results are presented in Figure-5.4.

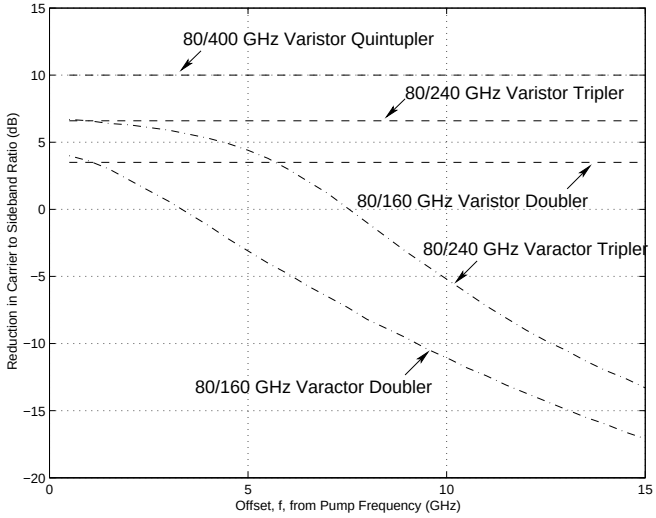

Figure 5.4: Plot of the degradation in carrier-to-sideband ratio for various frequency multipliers.

As an illustration, if the pump signal used to drive the 80/240 GHz varactor frequency tripler had 10 $K/\mu W$ noise in its sidebands then the sideband noise of the corresponding LO signal generated by the frequency multiplier at specified offset (say, 5 GHz) could be computed from the given plot as follows: The curve corresponding to the 80/240 GHz frequency tripler yields the value of the degradation in carrier-to-sideband ratio as 4.4 dB (for a 5 GHz

offset), thus implying 27.5 $K/\mu W$ noise in the output sideband, 5 GHz away from the carrier. Notice that for varactor type frequency multipliers, the curves cross the zero ordinate for sufficiently large offsets, implying that the output of the multiplier has less amplitude noise than the pump signal. This could be explained by the "filtering" action of the embedding networks far away from the design frequency. No such effect was observed for the varistor type frequency multipliers, in agreement with the fact that the embedding networks were all resistive and therefore not frequency selective.

5.4 Conclusion

The important topic of noise conversion in frequency multipliers was discussed in this chapter. While phase noise tends to be dominant close in to the carrier, the amplitude noise is dominant at larger offsets. The quasi-static approach, often useful to estimate the phase noise in a multiplier output was described. Subsequently, a method of estimating the sideband noise at large frequency offsets from the carrier was described together with relevant examples.

Experiments to measure the sideband noise (as a function of offset from the design frequency) at the input and output of a frequency multiplier remain to be performed. However measurements performed independently at National Radio Astronomy Observatory (NRAO) on the 211–275 GHz SIS mixer based receiver for the ALMA telescope indicates noticeable degradation in receiver temperature at intermediate frequencies in the range of 4–12 GHz. The up-conversion of sideband noise present in the YIG-oscillator source, by a chain of frequency multipliers used to derive the local oscillator

for the mixer, is thought to be the source of this degradation [159]. Two-tone harmonic balance simulations, similar to the ones described in Subsection-5.3.2, performed on real frequency multipler circuits have also yielded results commensurate with the ones presented in Figure-5.4 [159].

Chapter 6

Conclusions

Research over a five year period has culminated in the design, fabrication and evaluation of a fully integrable 80/240 GHz frequency tripler (Chapter-4) that clearly demonstrates the potential of planar and monolithic (MMIC) technology to provide viable LO sources in the 100–300 GHz frequency range. As a prelude to the above 80/240 GHz frequency tripler design, two hybrid-MIC frequency doublers (the 55/110 GHz and the 110/220 GHz frequency doubler) were designed, fabricated and evaluated (Chapter-2) to illustrate the limitations of "discrete diode package" based designs to provide viable and repeatable performance in this frequency range.

The more esoteric substrateless MMIC technologies (used predominantly to generate LO power beyond 300 GHz and well into the THz region) were avoided since they would yield extremely thin and rather large (and hence fragile) chips for outputs in the 100–300 GHz range.

This effort, the outcome of many fabricators, technicians, machinists, and other support personnel at NRAO and UVA, also resulted in the development of GaAs-membrane-on-quartz process for use in monolithic frequency multipliers. Several planar circuit structures like the MIM type integrated capacitors as well as planar spiral inductors on quartz substrates were designed, fabricated and evaluated in the W-band to gauge their suitability for frequency multiplier work. No previous published experimental data existed in this regard.

Analytical and simulation based study was performed to compare the sideband noise transfer characteristics of varactor and varistor mode frequency multipliers. The results are significant for receivers employing unbalanced mixers with large intermediate frequencies.

6.1 Overview

The important ideas and concepts presented in this dissertation, which the author considers new, novel, or unique are outlined below:

- **First fully integrable 80/240 GHz frequency tripler based on the GaAs-membrane-on-quartz substrate:** The extensive background research of Chapter-1 shows that although a few monolithic frequency multiplier designs based on thinned GaAs substrates exist for

this frequency range, this is the first reported effort to use a composite substrate (employing low dielectric quartz component as an alternative to thinning) to design monolithic frequency multipliers. This approach cirumvents both the dielectric loading as well as thermal dissipation issues.

- **First experimental study of the performance of planar capacitor and spiral inductor structures in the W-band:** This study (Chapter-3) showed that popular dielectrics used in MIM type planar capacitors (such as sputter deposited SiO_2, Chemical Vapor Deposited (CVD) SiO_2, and SiN) are all too lossy for use as reactance tuning components. They may however be employed in applications requiring large capacitance values (such as DC isolation capacitor). The design and measurements on planar spiral inductors indicated that with proper attention to design, the parasitic capacitance of the structure could be used to resonate the inductance at a certain frequency, providing a simple component that could serve to isolate across a certain frequency band while synthesizing the required inductive reactance at lower frequencies.

- **Use of thin 1 mil fused-quartz substrate:** The linear embedding circuitry for the 80/240 GHz frequency tripler was fabricated on 1 mil fused-quartz substrate. The thinnest reported quartz substrates used in frequency multipliers prior to this work were 2 mil thick.

- **A simple series planar impedance element synthesizing negative reactance:** The 80/240 GHz frequency tripler employs an air gap

coupled microstrip transmission line (Subsection-4.8.1) as a high quality series capacitive element. A good quality series capacitive element is generally the most difficult to synthesize, especially in millimeter- and submillimeter- wave applications. The zig-zag geometry of the air gap allows for a fairly large series capacitance to be synthesized. About 10–15 fF were synthesized across a 64 μm wide microstrip line on 1 mil fused-quartz substrate using an air gap of 2 μm.

- **Sideband noise transmission characteristics of frequency multipliers:** Analytical and simulation based study to characterize the sideband noise transmission characteristics of frequency multipliers was undertaken (Chapter-5) in order to compare the relative merits and demerits of varactor type versus varistor type frequency multipliers. This should be an important consideration for large intermediate frequency receivers employing unbalanced mixers.

6.2 Suggestions for Further Research

The following suggestions are offered to the future frequency multiplier researcher to help with good frequency multiplier designs at even higher frequencies:

- Fully integrated designs hold the key to good and repeatable performance, by allowing the designer to exercise a tighter control over circuit interactions (required for wide-bandwidth designs) as well as minimizing the unwanted parasitic variations found in hybrid-MIC designs (required for circuit repeatability). The shortcomings of the first iteration

of the 80/240 GHz frequency tripler could be traced back to the decision to fabricate the linear embedding circuits separate from the diode chip.

- Keep the design of the metal housing as simple as possible. Realize it as a two-piece split block to limit the number of assembly steps required to a bare minimum.

- Include the effects of machine tool sizes in the electromagnetic simulation model to accurately predict the multiplier mount behaviour. This is very important at millimeter- and submillimeter- wavelengths.

- Develop accurate models for performing accurate harmonic balance simulations on the non-linear element. Velocity saturation effects become significant and limit performance at higher frequencies.

- More innovative designs are possible with the development of suitable via-hole technology.

With photonic generation of local oscillator limited by the detector response speeds and noise, diode based frequency multipliers should continue to be the most reliable sources of local oscillator power for the foreseeable future.

Appendix A

Literature Review: Millimeter- and Submillimeter-wave Frequency Multipliers

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The abrupt-junction Schottky diode has been the single most important device for millimeter- and submillimeter-wave frequency multiplier work for quite some time. Up until the late 1980s and in the early 1990s, multipliers based on a whisker contacted Schottky diode were commonplace. In the later part of 1990s, these were replaced by discrete planar diodes in waveguides. This development was followed up by hybrid designs, wherein planar arrays

of diodes were incorporated into planar circuits. Currently, there is a push towards fully integrated monolithic multipliers, based on Schottky diodes.

Other technologies have emerged for frequency multiplier work, and some have been extremely successful, especially at frequencies below 100 GHz. In this section, a brief discussion of the various frequency multiplier technologies is presented and a comprehensive review of the state-of-the-art of frequency multiplier technology presented in a tabular form. Only *experimentally measured results* obtained from published literature are presented. The review was limited to a period starting 1991 to the present. Reviews of frequency multiplier technology for the period preceding this can be found elsewhere [3].

The information provided in the tables is organized as shown in Table-A.1.

Table A.1: Organization of information obtained from reviewed frequency-multiplier literature.

Type of Device	Symbols represent the active device, its circuit configuration and mount. A complete description of the symbols is presented in Table-A.2.
N	Multiplication factor, i.e. ×2 = Doubler, ×3 = Tripler, ×4 = Quadrupler etc.
Mount Type	Type of mount used. W/G = Waveguide, Hybrid-MIC = Individual devices or planar device arrays incorporated on to planar circuits, MMIC = Monolithic Microwave Integrated Circuit, GRID = Planar Grid, Quasi-optic = Quasi-optic arrangement for power coupling.
Number of devices	The number of devices used in the multiplier. Any specific device arrangement is noted where appropriate.
Output Frequency	Output frequency or frequency-range for the multiplier over which power, efficiency or conversion loss measurements are reported.
Maximum Output Power	The maximum output power measured over the *Output Frequency* range. Qualifiers, if any, are noted.
Notes	Other relevant information about the multiplier is recorded here. e.g. Efficiency, Conversion Loss or Gain, miscellaneous notes etc.
Ref.	The serial number of the literature reference as it appears in the bibliography from where the information was obtained.
Reference	First author and the year of publication of the literature reference.

Table A.2: Categorization of frequency multiplier technologies.

Symbol	Description of Configuration
F	FET/MESFET/HFET/HJFET in a hybrid microwave int. circuit (MIC) or monolithic microwave int. circuit (MMIC)
T	Hetero-junction barrier transistor incorporated into a hybrid MIC or MMIC
M	HEMT/PHEMT/RTHEMT incorporated into a hybrid MIC or MMIC
Mb	Balanced config. of HEMT/PHEMT/RTHEMT incorporated into a hybrid MIC or MMIC
S	Whisker contacted abrupt-junction Schottky diode in waveguide
sS	Abrupt-junction Schottky diode incorporated into a planar hybrid MIC
mS	Abrupt-junction Schottky diode incorporated into a planar MMIC
Sb	Balanced config. of planar abrupt-junction Schottky diodes in waveguide
sSb	Balanced config. of abrupt-junction Schottky diodes incorporated into a planar hybrid MIC
pS	Planar abrupt-junction Schottky diode in waveguide
pSb	Balanced config. of planar abrupt-junction Schottky diodes in waveguide
mSb	Balanced config. of abrupt-junction Schottky diodes incorporated into a planar MMIC
SG	Planar matrix of planar abrupt-junction diodes
QG	Planar matrix of quantum-well diodes
SGb	Planar matrix of a balanced config. of abrupt-junction diodes
NL	Non-linear transmission line, includes planar solitons
Q	Whisker contacted quantum-well diode in waveguide
sQ	Quantum-well diode incorporated into a planar hybrid MIC
mQ	Quantum-well diode incorporated into a planar MMIC
sD	Step-recovery diode incorporated into a planar hybrid MIC
pH	Planar hetero-junction barrier varactor diode in waveguide
sH	Hetero-junction barrier varactor diode incorporated into a planar hybrid MIC

A.1 Abrupt-junction Schottky diode

This kind of diode is a metal-semiconductor contact and it operates based on the energy barrier formed at the metal-semiconductor interface. Due to its high electron mobility, donor impurity doped (n-type) GaAs is most commonly used semiconductor for high frequency operation. The term "abrupt junction" refers to the uniform doping profile of the active n-doped GaAs. Such a diode may be operated as a non-linear resistive element (termed as varistor-mode operation) when in forward bias or as a non-linear capacitive reactance element (termed as varactor-mode operation) when in the reverse bias. In general varactor mode frequency multipliers have narrower bandwidths (about 10–15% fractional bandwidth) and high conversion efficiencies,

while varistor mode frequency multipliers have wider bandwidths (covering entire waveguide bands) but significantly lower efficiencies. Further details of Schottky diode operation may be found in Chapter-2.

The simplest form of abrupt-junction Schottky diode is a two-dimensional matrix of several small diameter metal anodes deposited on top of n-doped GaAs as shown in Figure-A.1. The n-doped layer resides on top of a n^{++}-doped buffer layer which is electrically contacted on the back side by and ohmic metal junction. One of the anodes is contacted by a very thin wire (or whisker) which forms the other terminal of the diode. Such a structure is referred to as a "whisker-contacted diode" or simply "whisker diode". Such diodes are usually mounted across the output waveguide in a frequency multiplier circuit. Some balanced whisker-contacted diode configurations can also be found in literature. Whisker contacted diodes have the lowest parasitics and are most suited for high frequency operation, well into the THz region. These diodes are however very difficult to assemble and lack ruggedness and repeatability due to the whisker structure.

Planar Schottky diodes, as illustrated in Figure-A.2, overcome the shortcomings of whisker diodes but inherently have higher parasitics due to their geometry as shown in the figure. Techniques to overcome the parasitics involve removal of semi-insulating GaAs substrate completely. Such planar designs have been reported to operate well into the THz frequency range. While this approach works well at higher frequencies, it results in large fragile structures at frequencies in the 100–300 GHz frequency range. The thin structure also causes thermal dissipation problems, particularly in large power handling applications. At these frequencies, the parasitics are themselves not as important as is the issue of dielectric loading of waveguide structures by the

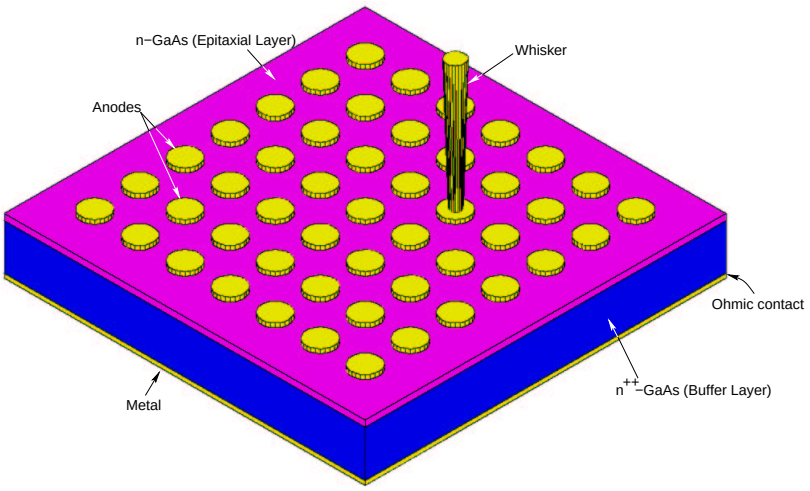


Figure A.1: Whisker contacted abrupt junction Schottky diode.

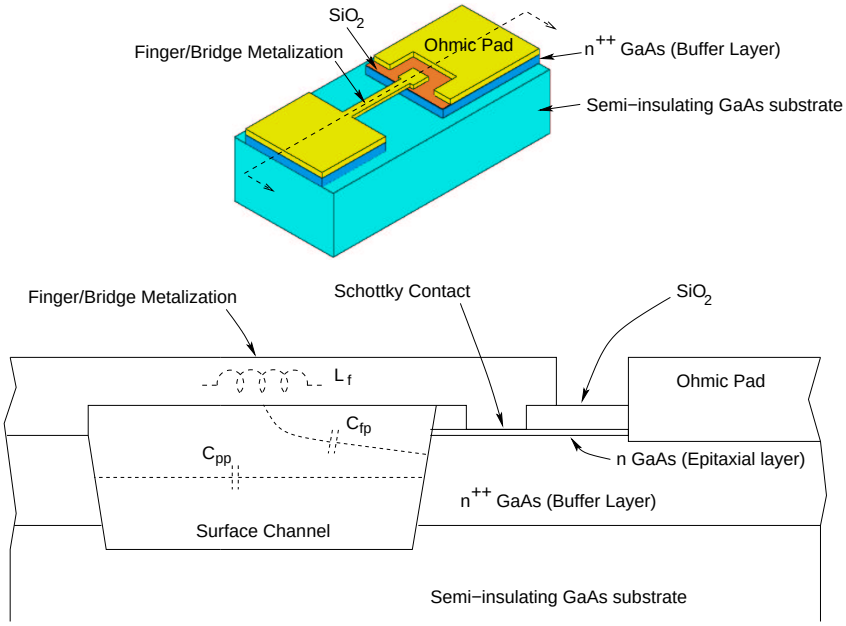


Figure A.2: Planarized abrupt junction Schottky diode.

high dielectric constant semi-insulating GaAs layer. Consequently techniques such as partial backside wafer thinning and GaAs-membrane-on-quartz type substrate (this work) have been successfully employed.

Another breed of Schottky diodes is a hybrid of the whisker contacted and planar diode approaches, where the ruggedness of a planar contact and low parasitics of a whisker diode are combined by fabricating an integrated whisker on the diode geometry of Figure-A.1 by the use of modern fabrication techniques. However, frequency multipliers based on such structures are rare to find [53].

Other two-terminal devices, similar to the abrupt Schottky junction diode with demonstrated non-linear behavior suitable for frequency multiplier application are the hyper-abrupt Schottky diode and the $Barrier-Intrinsic-N^{+}$ (BIN) structure and their variants.

Hyper-abrupt Schottky diodes are similar in structure to the abrupt-junction Schottky diodes except that the doping profile in non-uniform (but monotonic). Theoretically, the hyper-abrupt junction diodes have larger capacitance modulation than their abrupt-junction counterparts. Therefore frequency multipliers based on such structures should have higher frequency conversion efficiencies. Hyper-abrupt structures can also be found in a back to back configuration resulting in symmetric C-V characteristic, which finds application in idler-less odd-order frequency multipliers. Frequency multipliers based on these structures are however not very common.

Reports on the BIN (as well as the back-to-back BIN with symmetric C-V characteristic) can be traced up to the early 1990s. These structures have since diminished in importance, partly due to the low measured multiplication efficiencies caused by the losses in these multiple layer structures and partly due to the problems in controlling doping profiles while fabricating the devices.

Table-A.3 to A.6 summarize the state-of-the-art in Schottky diode based frequency multiplier technology.

Table A.3: State-of-the-art frequency multiplier performance (Schottky diode based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
mSb	×2	MMIC	2	735 - 850 GHz	1.1 mW 765 GHz	Max. Eff.=10% 765 GHz Substrate-less w/ frame	[34]	Chatto-padhyay 2002
mSb	×2	MMIC	2	368 - 424 GHz	8 mW 387 GHz	Max. Eff.=20% 387 GHz Substrate-less w/ frame	[35]	Schlecht 2001
mS	×2	MMIC	(1)?	94 - 116 GHz	0.6 mW (full-band)	Min. Eff.=3%	[36]	Ermak 2001
mSb	×3	MMIC	2	1126 GHz	80 μW 195 μW (at 120K) 250 μW (at 50K)	Max. Eff.=0.9% 3-dB BW=3.5% Membrane w/o frame "MOMED"	[37]	Maestrini 2001
mSb	×3	MMIC	2	75 - 110 GHz	-3.7 - 2 dBm	Eff.=1.5% (full-band)	[38]	Morgan 2001
mSb	×2	MMIC	1,2	2550 GHz	0.1 μW	"MOMED"	[39]	Maiwald 2001
sSb	×3	Hybrid-MIC in W/G	2 in single package	210 GHz	2 mW	Anti-series, inhomogeneously doped, Mechanical tuner	[40]	Krach 2000
mS	×2	MMIC	2	68 - 78 GHz	71 mW 74 GHz	Min. Conv. Loss= 8.4 dB 74 GHz	[41]	Guan-Leng 2000
mS	×2	MMIC	2	72 - 73 GHz		Conv. Loss= 6.4 dB	[41]	Guan-Leng 2000
?S?	×2	?	?	75 - 110 GHz	4 dBm (full-band)	Conv. Loss=16 dB	[42]	Tao 2000
mSb	×2	MMIC	(4)?	74 GHz	115 mW	Max. Eff.=12.5% 3-dB BW=12.5%	[43]	Papapoly-merou 2000
mSb	×3	MMIC	2	230 - 325 GHz	5 - 7 mW 300 GHz?	Max. Eff.=11% 300 GHz? Min. Eff.=1% (full-band)	[44]	Erickson 2000

Table A.4: State-of-the-art frequency multiplier performance (Schottky diode based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
sS	×2	Hybrid-MIC	1	62 GHz	10.8 dBm	Conv. Loss=12 dB	[45]	Le Bras 1999
sSb	×2	Hybrid-MIC	6	80 GHz	112.5 mW	Max. Eff.=48% 3-dB BW=17%	[46]	Porter-field 1999
sSb	×2	Hybrid-MIC	6	80 GHz	175.2 mW (at 14K)	Max. Eff.=61% (at 14K)	[46]	Porter-field 1999
mS	×2	MMIC	?	5.6 - 8.5 GHz	16 dBm	Conv. Loss=0 dB MIC includes cascaded Amp.	[47]	Rasa 1999
Mb	×4	Hybrid-MIC	4 per stage	300 GHz	6.1 mW	×2-×2 cascade	[48]	Newman 1999
mS	×2	MMIC in W/G	2	80 GHz	72 mW, 93 mW	Eff.=16.3% 80 GHz 3-dB BW>10 GHz	[49]	Papapoly-merou 1999
mS	×2	MMIC in W/G	2	71.5 GHz	11 mW w/ an input of 50 mW	Eff.=21.5% 70 GHz 3-dB BW>6 GHz On-wafer results	[49]	Papapoly-merou 1999
mS	×2	MMIC	(1)?	320 GHz	420 μW	Max. Eff.=2.8%	[50]	Bruston 1998
(p?)S	×2	(W/G)?	(1)?	150 GHz	?	Max. Eff.=40%	[51]	Simon 1998
(p?)S	×3	(W/G)?	(1)?	267 GHz	5.6	Max. Eff.=19%	[51]	Simon 1998
(p?)S	×3	(W/G)?	(1)?	300 GHz	5.5	Max. Eff.=16%	[51]	Simon 1998
(p?)S	×3	(W/G)?	(1)?	480 GHz	2 mW	Max. Eff.=8%	[51]	Simon 1998
SG	×2	Quasi-optic Grid	144	1 THz	10.3 mW 24 mW (for pulsed I/P)	Max. Eff.=0.17%	[52]	Mousse-ssian 1998
pS	×3	W/G	1	245 GHz	3.3 mW Device out--put is 8.5 mW	Eff.=11% Integrated contact	[53]	Thornton 1998
pS	×3	W/G	2	270 GHz	Device out--put is 15 mW	Eff.=5% Integrated contact	[53]	Thornton 1998

Table A.5: State-of-the-art frequency multiplier performance (Schottky diode based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
sS	×2	Hybrid-MIC	?	76 GHz	0 dBm	×2-Amp. cascade on chip	[54]	Ohashi 1998
mS	×2	MMIC	2	W-Band	66 mW Max. 76.3 GHz	Max. Eff.=22.9% 3-dB BW>8 GHz Finite ground plane lines	[55]	Papapoly-merou 1998
mS	×2	MMIC	2	D-Band	100 μW 160 GHz	Max. Eff.=0.85% Finite ground plane lines	[55]	Papapoly-merou 1998
sS	×2	Hybrid-MIC?	1?	200 GHz	5 mW	Eff.=12.5%	[56]	Chih-I 1998
mS	?	MMIC	?	70 - 80 GHz	93 mW Max.	Eff.=26% Max.	[57]	Brauchler 1997
sS	×2	Quasi-optic	(1)?	600 GHz	1 mW	Max. Eff.=2%	[58]	Kim 1997
mS	×2	MMIC	(1)?	76 GHz	20 mW minimum	Med. Power. Amp. -×2 Cascade on chip	[59]	Stotz 1997
Hyper-abrupt Schottky diode	×3	Quasi-optic Grid	4× 4 matrix of anti-series pairs	15 GHz	40 mW	Commercial diode package from α-Industries	[60]	Kurtz 1997
sS	×2	W/G	1	200 GHz	2.6 mW	Eff.=7.1% Mech. Sliding Back-shorts	[61]	Louhi 1997
(S?)	×3	W/G	1?	804 GHz	250 μW		[62]	Crowe 1996
(S?)	×2	W/G	1?	262 GHz	10 mW		[62]	Crowe 1996
sSb	×3	Hybrid-MIC in W/G	2 in single package	220 GHz	700 μW	Max. Eff.=7% Mechanical tuner for I/P and O/P	[63]	Choudhury 1994
sSb	×4	Hybrid-MIC	(1)?	37.5 GHz	75 mW		[64]	Zhang 1994
sS	×2	MMIC	?	16 - 40 GHz	6 dBm Max.	Varistor mode wide-band output Finite ground plane lines On-chip results	[65] [66]	Maas 1994

Table A.6: State-of-the-art frequency multiplier performance (Schottky diode based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
mS	?	MMIC	?	Ku-Band	3 dBm over 30% BW		[67]	Westhuizen 1994
(sS?)	×4	?	?	56 GHz	100 mW		[68]	Piloni 1994
mSb	×3	MMIC	Four 6 × 12 arrays	97 GHz	19 dBm	On-wafer results	[69]	Cohn 1994
sSb	×2	Hybrid-MIC?	2 anti-serial	7.2 GHz	15.5 dBm		[70]	Filipovic 1994
mS	×2	MMIC	1	94 GHz	65 mW?	Eff.=19.7%	[71]	Seng-Woon 1993
S	×4	Quasi-optic	1 2 4	580 GHz 580 GHz 580 GHz	20 μW 15 μW 22 μW		[72]	Steup 1993
(s?)S	×2	?	?	160 GHz	22 mW(300K) 30.7 mW(77K)		[73]	Louhi 1993
(sSb?)	×2	Hybrid-MIC?	4	174 GHz	55 mW	Max. Eff.=25%	[74]	Rizzi 1993
SG (mS?)	×2	Quasi-optic Grid	1000s	66 GHz	2.1 W		[75]	Qin 1993
SG (mS?)	×3	Quasi-optic Grid	1000s	99 GHz	5 W		[75]	Qin 1993
Gb	×2	Quasi-optic Grid	1760	66 GHz	2.1 W	Max. Eff.=7.5% BNN^+ structure	[76]	Xiaohui 1993
(S?)	×3	W/G	(1)?	750 GHz	120 μW	Eff.=0.8%	[77]	Rydberg 1992
mS	×2	MMIC	1	93 GHz	30 mW		[78]	Hegazi 1991
mSb	×2	MMIC	4-junc. diode-pairs	6 - 18 GHz GHz	11 dBm	Eff.=12.6% Coplanar W/G lines	[79]	Bitzer 1991
mSb	×2	MMIC	4-junc. diode-pairs	10 - 27 GHz	11 dBm	Eff.=12.6% Coplanar W/G lines	[79]	Bitzer 1991
(S?)	×4	MMIC	?	44.5 GHz	0 dBm	Conv. Loss=20 dB ×2-×2 cascade	[80]	Creamer 1991

A.2 Other Diodes

Other two-terminal devices with demonstrated non-linear behavior suitable for frequency multiplier application are the Integrated Series IMPATT structure (ISIS), the Resonant Tunneling Diode (RTD) or the quantum-well diode structure and the Hetero-junction Barrier Varactor (HBV).

As is the case with hyper-abrupt junction diodes and BIN structures, reports of the ISIS structures can be traced up to the early 1990s. These structures have since diminished in importance, and find use only in niche applications.

The quantum-well diode structure is a negative resistance device commonly used in fundamental millimeter-wave oscillators. This double barrier structure also exhibits a polarity-symmetric negative resistance region that has been exploited for odd-order harmonic generation.

The HBV structure, invented in 1989, has been recently developed extensively for application in odd-order frequency multipliers (predominantly frequency triplers). The structure, in its discrete form, is illustrated in Figure-A.3. Due to the geometric symmetry of the structure, it exhibits a symmetric C-V characteristic which makes it suitable for odd-order frequency multiplier design. Planar versions of the HBV structure, as illustrated in Figure-A.4, comprise of a series of back-to-back HBV structures having lower device capacitances (making them suitable for high frequency applications) and theoretically a larger power handling capability. The reported experimental power outputs of HBV based frequency multipliers have however been lower than that of the Schottky diode based frequency multipliers, perhaps due to the larger losses associated with the multiple stack HBV structures.

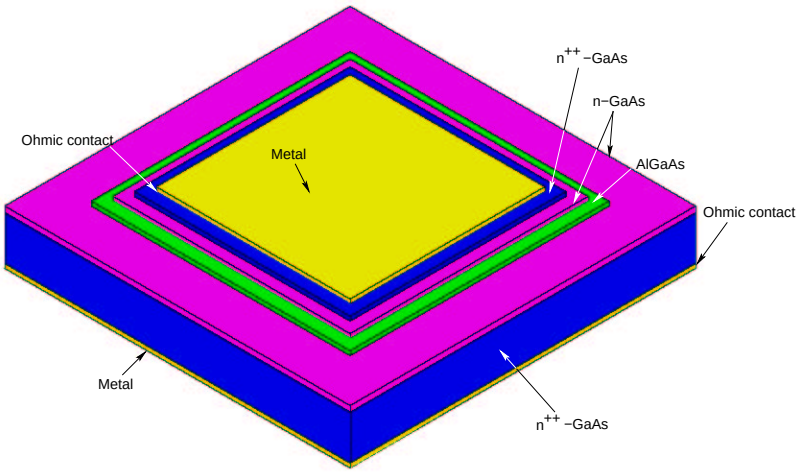


Figure A.3: Discrete hetero-junction barrier varactor diode.

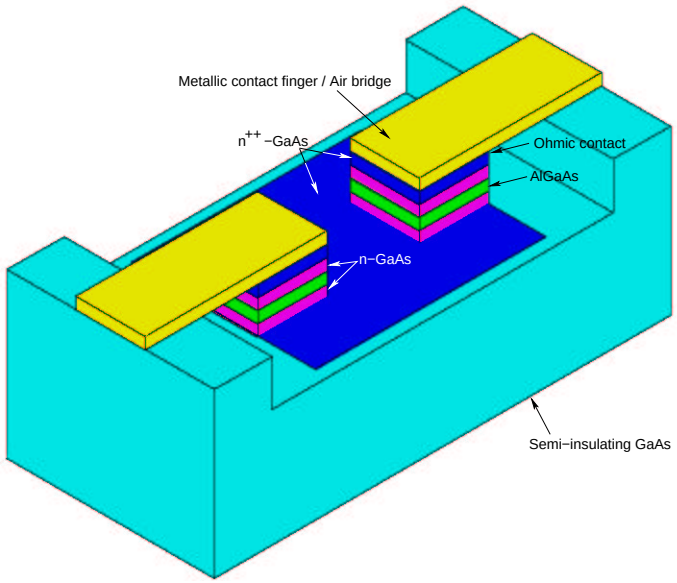


Figure A.4: Planarized hetero-junction barrier varactor diode.

Table-A.7 and A.8 summarize the state-of-the-art in quantum-well diode and hetero-junction barrier varactor based frequency multipliers.

Table A.7: State-of-the-art frequency multiplier performance (Other two-terminal device based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
pH	×3	W/G	1	290 GHz	5 mW	Mech. tuned W/G	[81]	David 2001
pH	×3	(WG)?	1	221 GHz	7.1 mW	Max. Eff.=7.9% 3-barrier device on Cu-substrate	[82]	Dillner 2000
pH	×3	(W/G)?	?	221 GHz	7.1 mW	Eff.=7.9% Mech. tuned W/G?	[83]	Dillner 2000
pH	×3	W/G	1	247.5 GHz	9.55 mW	Eff.=10.7% Mech. tuned W/G	[84]	Melique 2000
mQ	×3	MMIC	1	210 GHz	10 mW	Eff.=13.5% Mech. tuned W/G SBV-device	[85]	Meola 2000
pH	×3	W/G	1	250 GHz	9 mW	Eff.=12% Mech. tuned W/G	[86]	Melique 1999
pH	×3	(WG)?	(1)?	234 GHz	3.6 mW		[87]	Kollberg 1998
pH	×3	MIC	2	216 GHz	5 mW	Eff.=5.4%	[88]	Melique 1998
(pH?)	×3	?	?	261 GHz	2 mW		[89]	Stake 1998
IMPATT	×2	?	?	210 GHz	1 mW	Self-pumped	[90]	Bohm 1998
pH	×3	W/G	4-barrier	252 GHz	2 mW	Eff.=25%	[91]	Jones 1997
pH	×3	W/G	?	Ka-Band	20 dBm 40.35 GHz	Conv. Loss= 7 dB	[92]	Krishna-murthy 1996
sH	×3	Micro-strip	?	Ka-Band	10.8 dBm 40.35 GHz	Conv. Loss= 11 dB	[92]	Krishna-murthy 1996
sQ	×3	Hybrid-MIC?	?	60 GHz	22 dBm	MSQBV-device	[93]	Rahal 1995
sQ	×3	Hybrid-MIC?	?	90 GHz	3 dBm	MSQBV-device	[94]	Rahal 1995

Table A.8: State-of-the-art frequency multiplier performance (Other two-terminal device based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
(Q?)	×3	W/G	1	93 GHz	19.6 dBm		[95]	Rahal 1995
Q	×5	W/G	(1)?	148 - 187 GHz	130 μW 171.5 GHz 143 μW 172.5 GHz	Max. Eff.=0.78% 172 GHz SBV-device	[96]	Raisanen 1995
QG	×3	Quasi-optic Grid	?	99 GHz	1.25 W	MQBV-device	[97]	Liu 1993
QG	×3	Quasi-optic Grid	?	99 GHz	5 W	SQBV-device	[97]	Liu 1993
SG	×2	Quasi-optic Grid	(many)?	66 GHz	2.4-2.6 W	Eff.>10% BNN^+ structure	[98]	Liu 1992
QG	×3 ?	Quasi-optic Grid	1300	99 GHz	3.8-10 W	Eff.=1.7-4% SQBV-device	[98]	Liu 1992
sD	×6	Hybrid-MIC	1	10.5 GHz	12 dBm		[99]	Ramana 1992

A.3 Three-terminal Devices

Field Effect Transistors (FETs), MESFETs, Hetero-structure FETs (HFETs), Hetero-structure Junction FETs (HJFETs), Hetero-junction Bipolar Transistors (HBTs),High Electron Mobility Transistors (HEMTs), Pseudomorphic HEMTs (PHEMTs), and the doped channel Pseudomorphic HFETs (PHFETs) have all been used in MIC and MMIC type frequency multipliers. Table-A.9 to A.11 summarize the state-of-the-art in three-terminal device based frequency multipliers.

Table A.9: State-of-the-art frequency multiplier performance (Three-terminal device based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
M	×2	MMIC	1	76.5 GHz	9 dBm	Conv. Gain=1 dB PHEMT-device	[100]	Werthof 2001
M	×2	MMIC	(1)?	164 GHz	5 dBm	Conv. Loss=2 dB 3-dB BW=8.5% HEMT-device	[101]	Radisic 2001
M	×3	MMIC	1	38 GHz	3.1 dBm	Max. Eff.=11% PHEMT-device	[102]	Boudiaf 2000
M	×2	MMIC	1	48 - 60 GHz	6 dBm	Conv. Gain=1 dB HEMT-device	[103]	Fager 2000
M	×2	MMIC (3-D fab.)	?	65 GHz	5.5 dBm	Conv. Loss= 8.5 dB PHEMT-device	[104]	Piernas 2000
M	×3	MMIC	1	24 - 27 GHz	4 dBm Max.	Conv. Loss= 6-8 dB PHEMT-device	[105]	Verver 2000
M	×3	MMIC	1	76.5 GHz	7 dBm Max. (saturated)	Min. Conv. Loss= 4.3 dB PHEMT-device	[106]	Campos-Roca 2000
T	×3	MMIC	?	25.5 - 31.5 GHz	>10 dBm (full-band)	Conv. Loss <5 dB	[107]	Beaulieu 2000
M	×2	MMIC	1	?	7 dBm	3-dB BW=25% MIC includes cascaded Amp. HEMT-device	[108]	Zirath 1999
?	×2	MMIC	?	76 GHz	10.4 dBm	MIC includes cascaded Amp.	[109]	Maruhashi 1999
M	×2	MMIC	1	1.4 GHz	-8.5 dBm	Conv. Gain= 1.5 dB RTHEMT-device	[110]	Kawashima 1999
M	×2	MMIC	?	76 GHz	10 dBm	Min. Conv. Loss= 4 dB PHEMT-device	[111]	Campos-Roca 1999
M	×4	MMIC	?	76 GHz	4 dBm	Min. Conv. Loss= 7.5 dB PHEMT-device	[111]	Campos-Roca 1999
M	×4	MMIC	(2)?	90.8 - 94.3 GHz	1.6 dBm (full band)	HBT VCO-HBT Amp. -×2-HEMT Amp.-×2 Cascade on chip HEMT-device	[112]	Wang 1998

Table A.10: State-of-the-art frequency multiplier performance (Three-terminal device based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
M	×3	MMIC	2	Q-Band	12 dBm	Input Amp. over-drives Class-A Amp. PHEMT-device	[113]	Fudem 1998
M	×3	MMIC	2	W-Band	5 dBm	Input Amp. over-drives Class-A Amp. PHEMT-device	[113]	Fudem 1998
T	×2	?	?	54.5 GHz	10 mW	Conv. Loss <12 dB 3-dB BW=7.4%	[114]	Bruce 1998
F	×2	MMIC	(1)?	V-Band	16.8 dBm	Conv. Gain= 9.1 dB BW=4 GHz MIC includes Cascaded Amp. HJFET-device	[115]	Inoue 1997
M	×2	MMIC	(1)?	Ka-Band	-2 dBm 26 GHz	HEMT-device Amp.-×2 cascade	[116]	Tran 1996
M	×2	MMIC	(1)?	V-Band	5 dBm 54 GHz	HEMT-device Amp.-×2 cascade	[116]	Tran 1996
M	×4	MMIC	(1)?	60 GHz	-5 dBm	Conv. Loss= 5 dB HEMT-device	[117]	Shirakawa 1996
M/F	×2	MMIC	?	40 GHz	2 dBm	Conv. Loss= 3-4 dB HEMT-device & MESFET-device	[118]	Kangas-lahti 1996
M	×3	MIC	1	22.8 GHz	-7 dBm	HEMT-device	[119]	Zhang 1996
M	×4	MMIC	(1)?	94 - 95 GHz	3 dBm	VCO MIC-×4 MIC-3-stage Amp. MIC cascade HEMT-device	[120]	Wang 1995
F	×2	MMIC	1	60 GHz	5.5 dBm	Conv. Loss= 1.5 dB HJFET-device	[121]	Funabashi 1995
M	×2	MMIC?	?	60 GHz	-5 dBm	HEMT-device	[122]	Kawasaki 1994

Table A.11: State-of-the-art frequency multiplier performance (Three-terminal device based).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
?	×2	MMIC	?	94 GHz	95 mW	Amp.-×2 cascade on chip	[123]	Ho 1994
M	×4	MMIC	(1)?	94 - 98 GHz	?	×2-Buff. Amp.-×2 cascade HEMT-device	[124]	Wang 1994
F	×2	MMIC	?	88 - 96 GHz	-5 dBm 90 GHz	Eff.=2-3% (full-band) HFET-device	[125]	Zirath 1993
M	×2	MMIC	?	130.5-132.8 GHz	-12 dBm (full-band)	HEMT-device	[126]	Kwon 1992
Mb	×2	MMIC	2	42 GHz	4 dBm	Conv. Loss= 1 dB at 40 GHz PHEMT-device	[127]	Angelov 1992
F	×2	Hybrid-MIC	1	36 GHz	-5 dBm?		[128]	Tuko 1992
F	×2	Hybrid-MIC	2	36 GHz	3 dBm?		[128]	Tuko 1992
F	×2	MMIC	?	24 GHz	8.25 dBm	Buil-in leveler MESFET-device	[129]	Piloni 1992
M	×2	MMIC	?	180 GHz	-6 dBm	Conv. Loss= 6 dB HEMT-device	[130]	Kwon 1991
M	×2	MMIC	?	45 GHz	15 dBm	×2-MESFET Amp. cascade on chip PHEMT-device	[131]	Khanna 1991

A.4 Distributed Element Structures

Planar non-linear lines have been demonstrated to operate as harmonic generators for quite some time. Careful design can also lead to soliton propagation along these non-linear transmission lines which result in harmonic power generation as well. The non-linear transmission lines are generally transmission line structures (like coplanar waveguides) loaded periodically with non-linear devices (such as Schottky diodes). Table-A.12 summarizes the state-of-the-art for such non-linear transmission line structures.

Table A.12: State-of-the-art frequency multiplier performance (Distributed element structures).

Type of Device	N	Mount Type	Number of Devices	Output Frequency	Maximum Output Power	Notes	Ref.	Reference
NL	×3	MMIC	8 HBVs	60 GHz		Max. Eff.=1% 30% BW	[132]	Fernandez 2001
NL	×3	Hybrid-MIC	15 HBVs	130.5 GHz	10 dBm	Max. Eff.=7% 3-dB BW=10%	[133]	Hollung 2000
Gyrofrequency multiplier	×6	Tube	-	17.23 GHz	3.5 kW		[134]	Balkcum 1995
NL	×2	Hybrid-MIC?	?	52 - 63.1 GHz	17.4 dBm (full-band)		[135]	Carman 1992
NL	×3	Hybrid-MIC?	?	81 - 108.8 GHz	12.8 dBm (full-band)		[135]	Carman 1992
NL Soliton	×2	Hybrid-MIC?	20	26 - 40 GHz	8 dBm (full-band) 11.7 dBm Max.		[136]	Carman 1991
NL Soliton	×2	Hybrid-MIC?	10	26 - 40 GHz	8 dBm (full-band) 12.7 dBm Max.		[136]	Carman 1991

Appendix B

Mask-set Drawings

The drawings of the mask-sets used in the photolithographic fabrication of quartz based circuits (for the 55/110 GHz and 110/220 GHz frequency doublers and the 80/240 GHz frequency tripler) are presented in this appendix. Also included is the artwork used for the fabrication of printed circuit board for the DC biasing circuit of the 80/240 GHz frequency tripler.

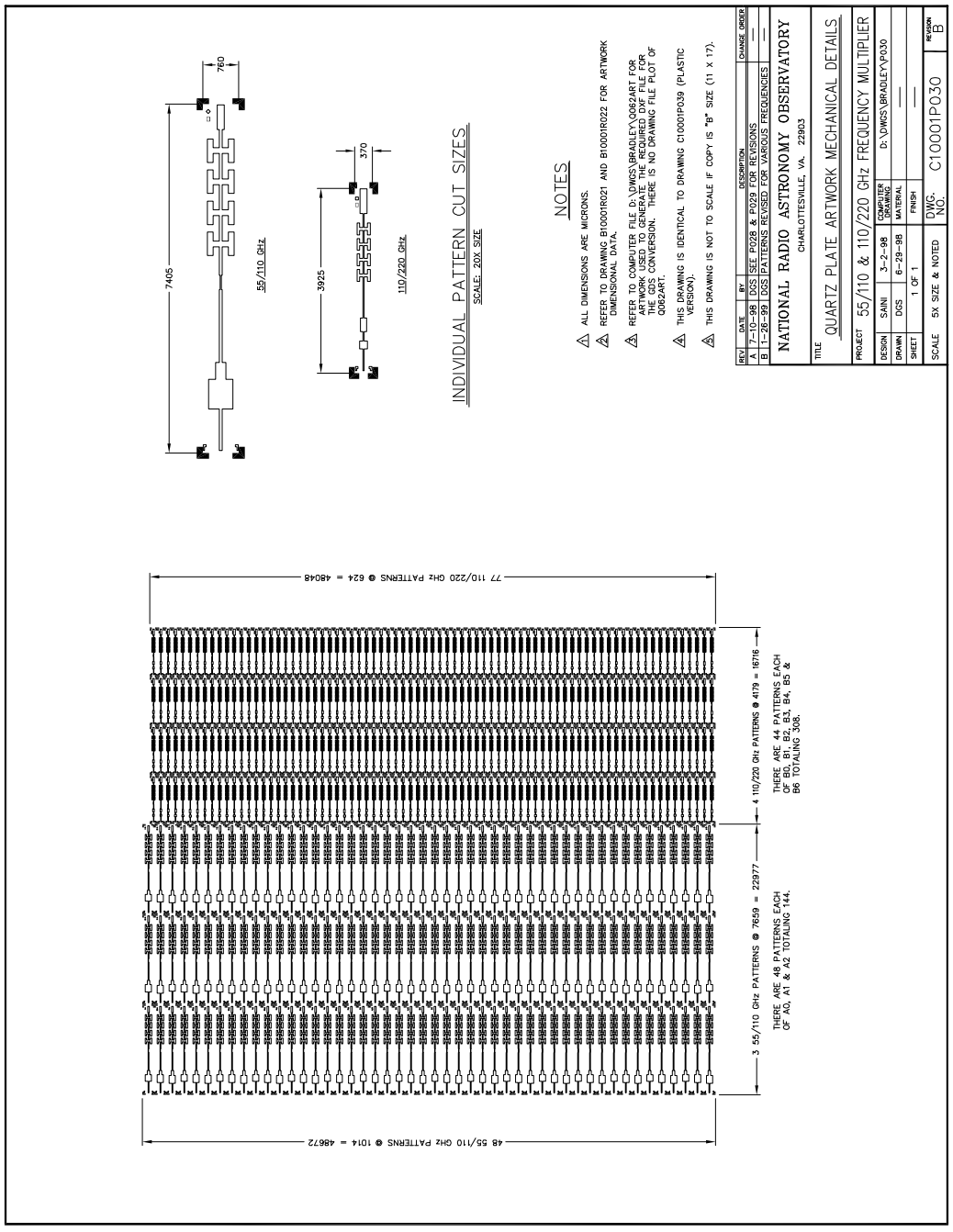


Figure B.1: Details of the mask set used in the fabrication of quartz circuits for the 55/110 GHz and 110/220 GHz frequency doublers.

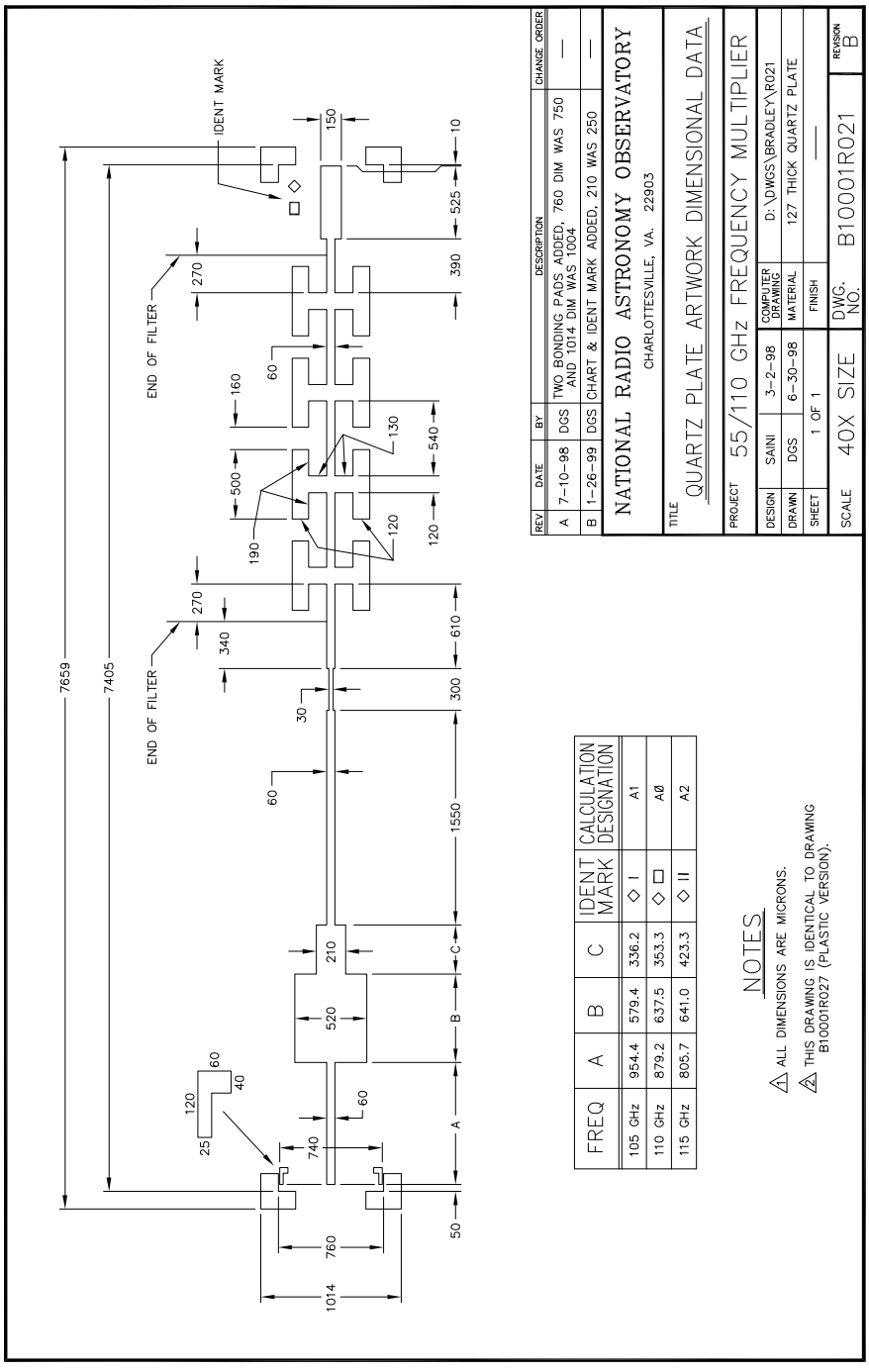
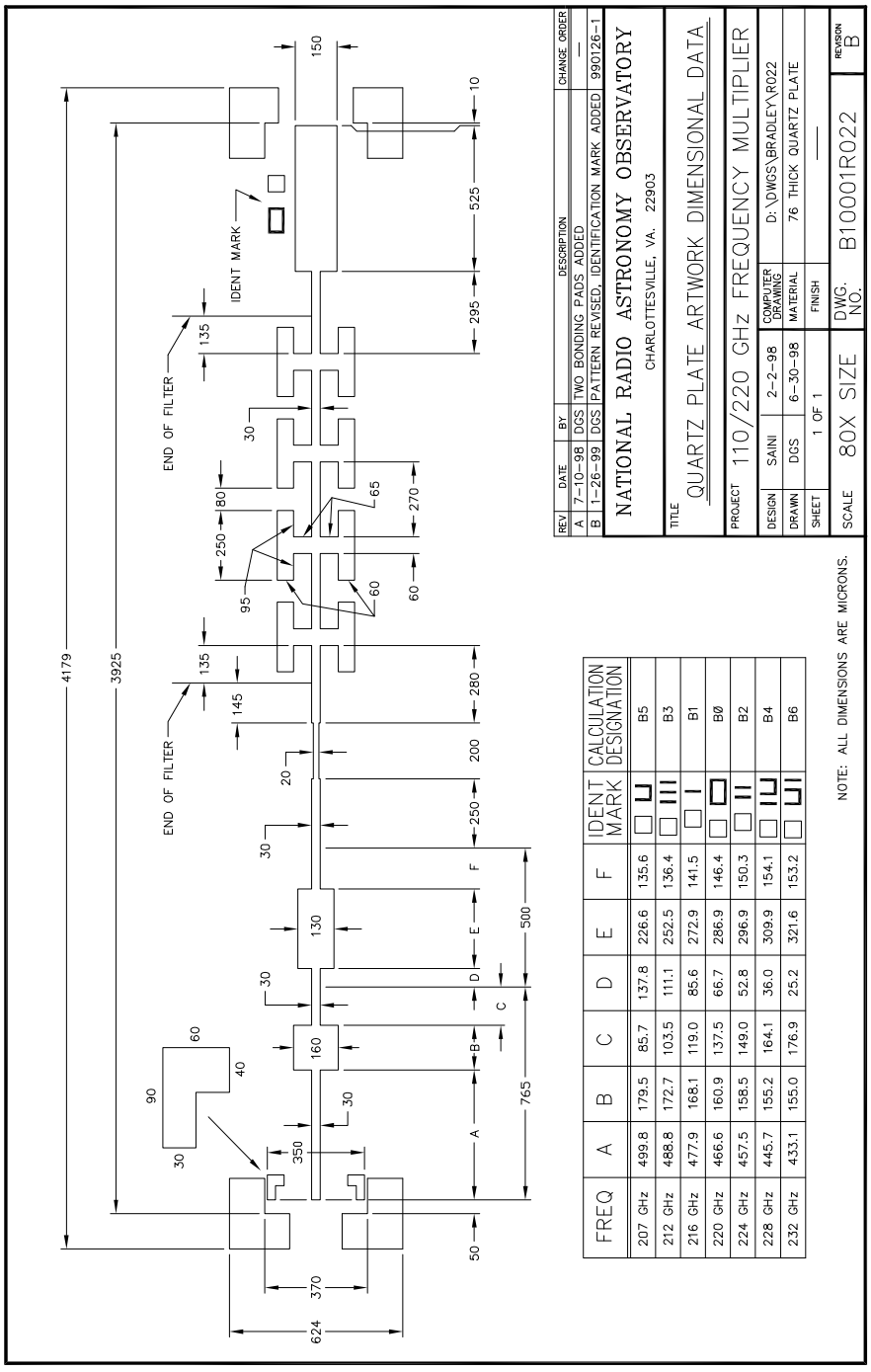


Figure B.2: Dimensional details of the artwork representing the metalization pattern on an individual quartz circuit used in the 55/110 GHz frequency doubler.



FREQ	A	B	C	D	E	F	IDENT MARK	CALCULATION DESIGNATION
207 GHz	499.8	179.5	85.7	137.8	226.6	135.6		B5
212 GHz	488.8	172.7	103.5	111.1	252.5	136.4		B3
216 GHz	477.9	168.1	119.0	85.6	272.9	141.5		B1
220 GHz	466.6	160.9	137.5	66.7	286.9	146.4		B0
224 GHz	457.5	158.5	149.0	52.8	296.9	150.3		B2
228 GHz	445.7	155.2	164.1	36.0	309.9	154.1		B4
232 GHz	433.1	155.0	176.9	25.2	321.6	153.2		B6

Figure B.3: Dimensional details of the artwork representing the metalization pattern on an individual quartz circuit used in the 110/220 GHz frequency doubler.

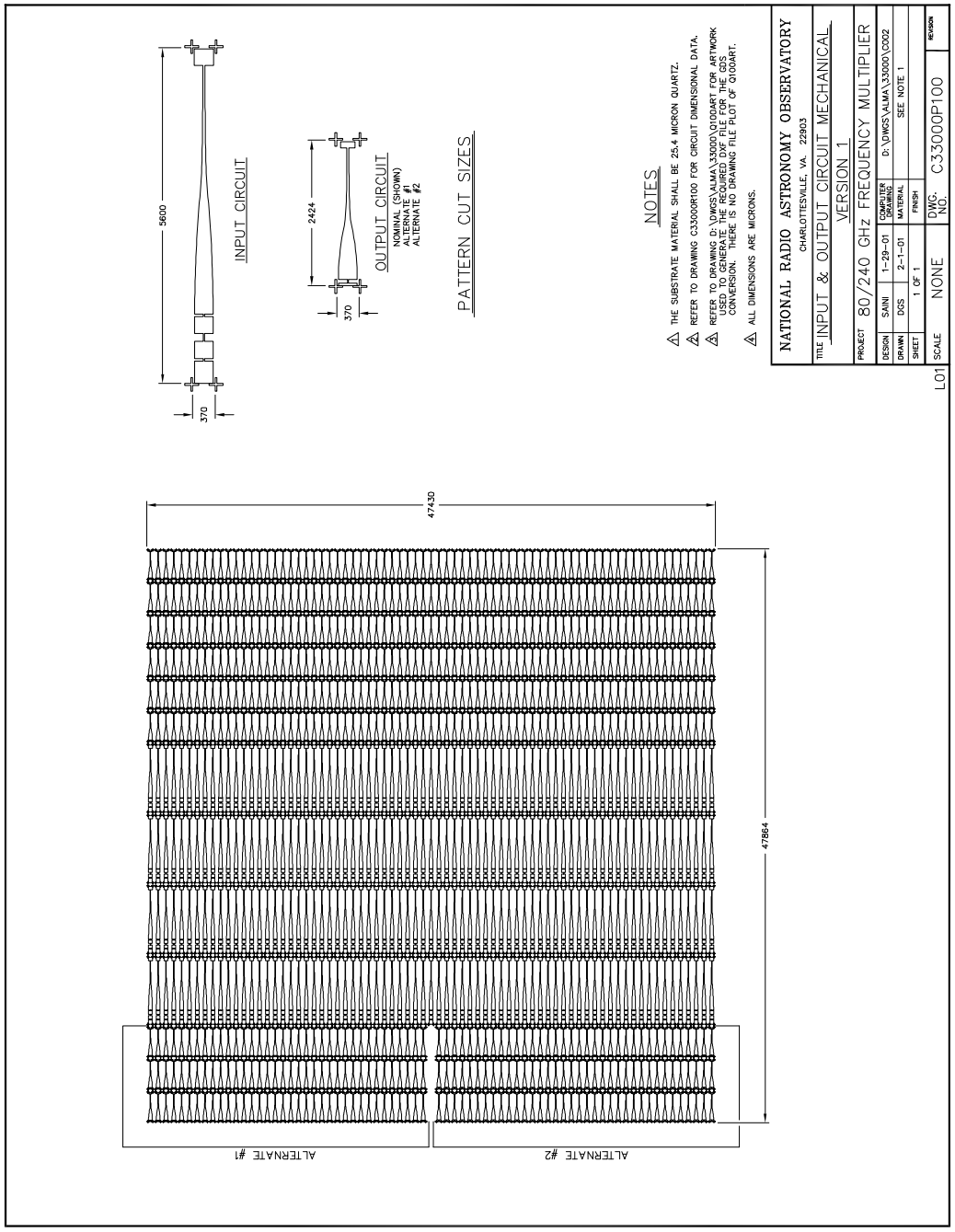


Figure B.4: Details of the mask set used in the fabrication of input and output quartz circuits for the 80/240 GHz frequency tripler (version 1).

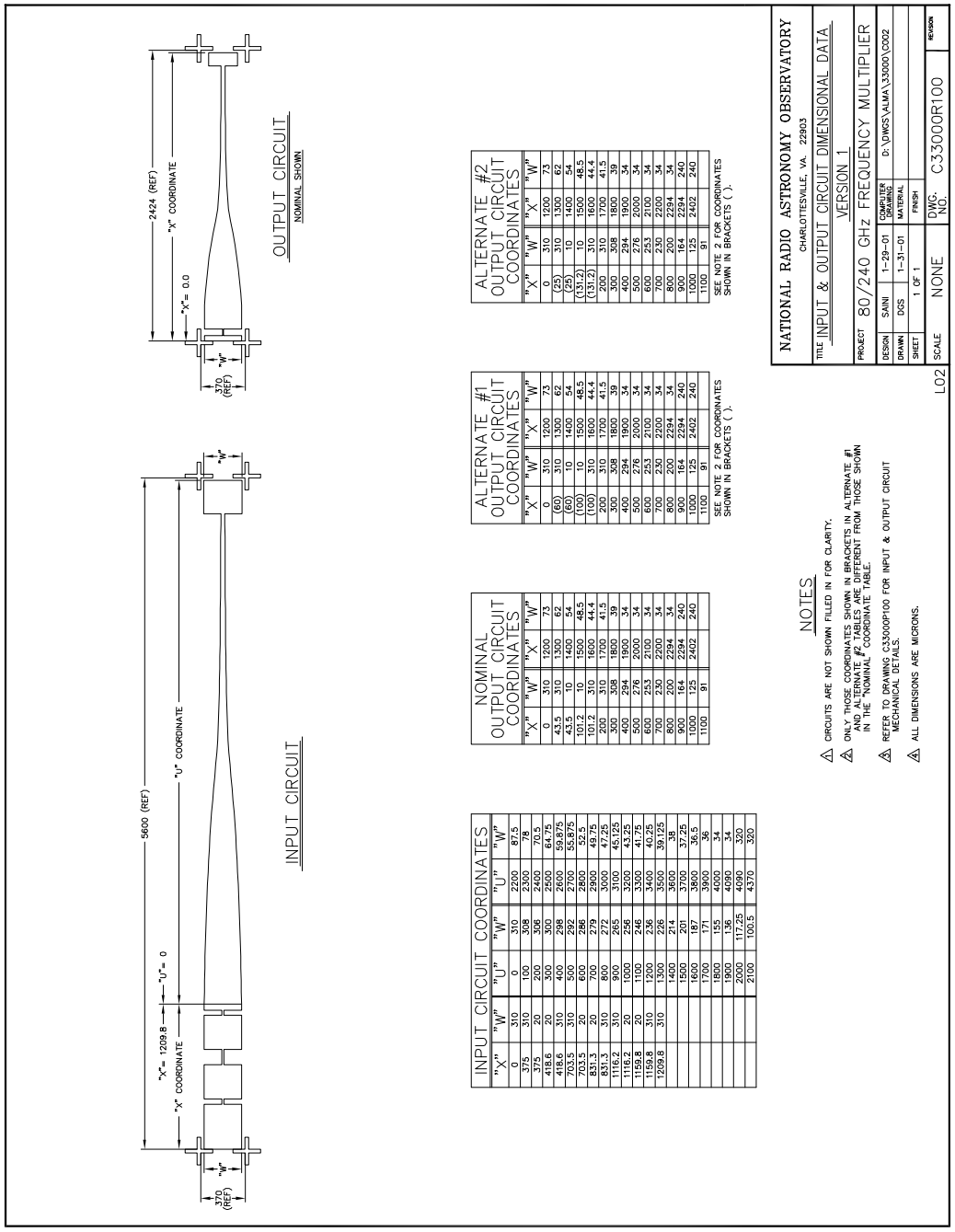


Figure B.5: Dimensional details of the artwork representing the input and output metalization patterns for the quartz circuits used in the 80/240 GHz frequency tripler (version 1).

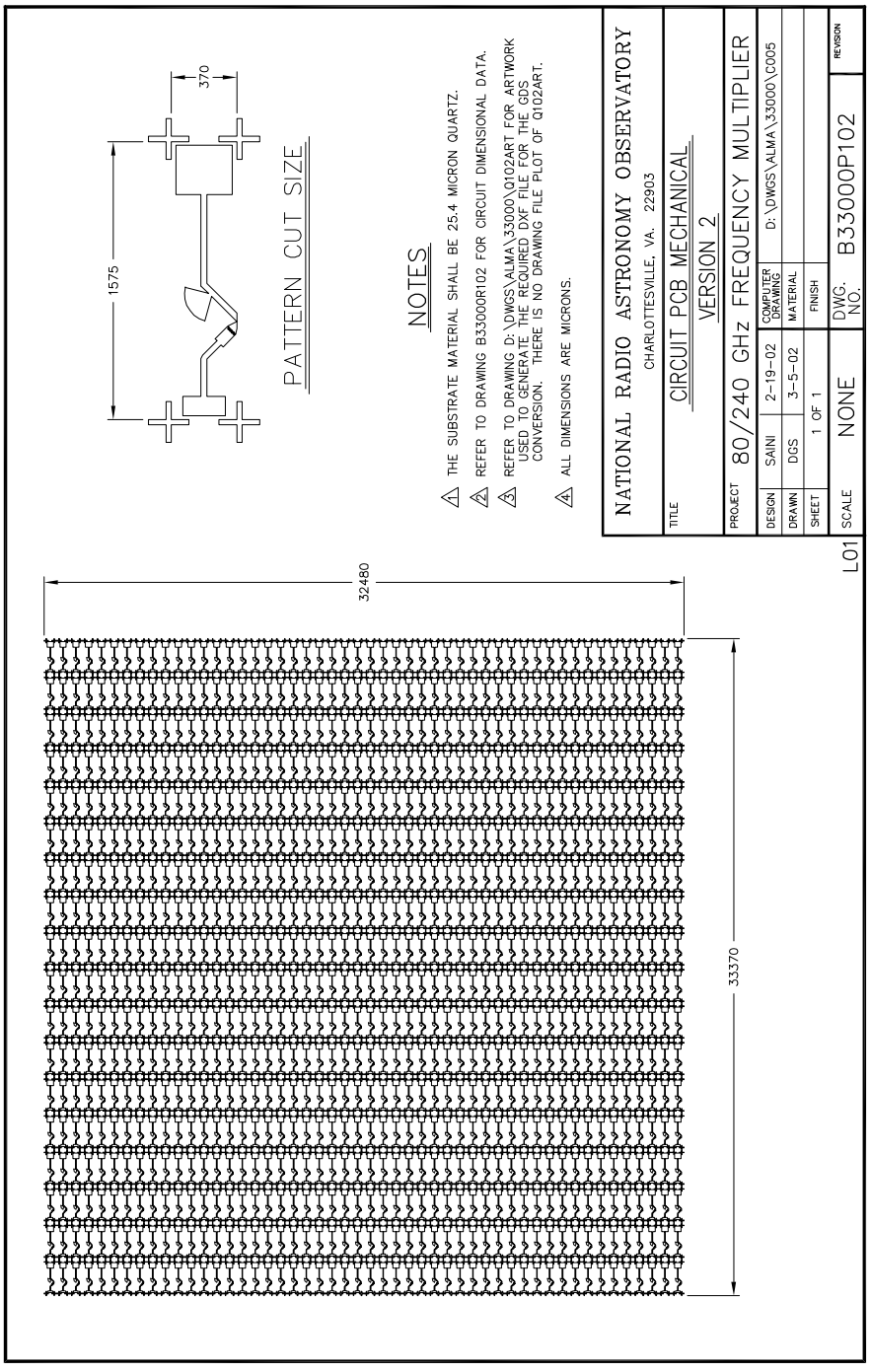


Figure B.6: Details of the mask set used in the fabrication of quartz circuits for the 80/240 GHz frequency tripler (version 2).

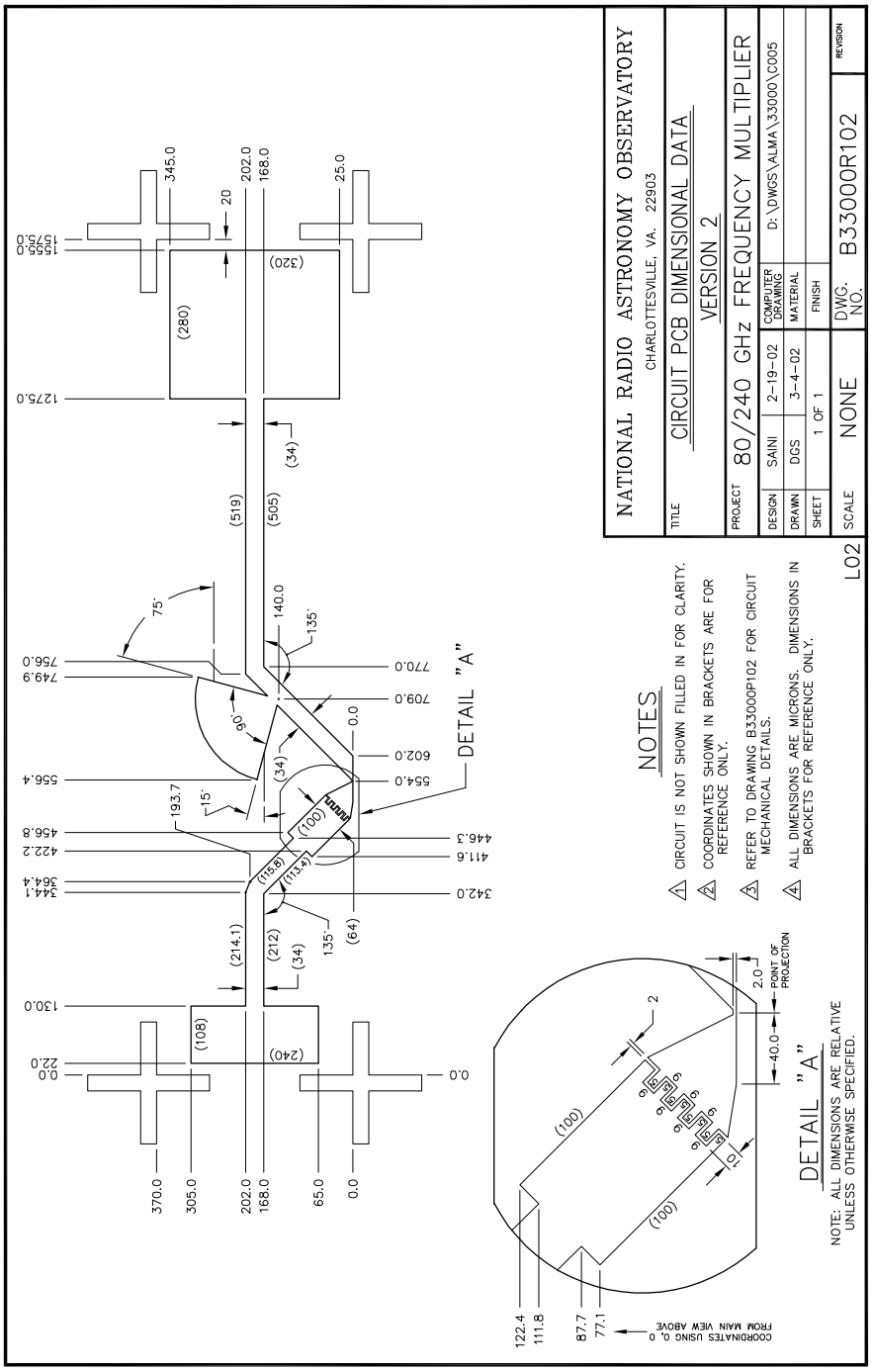


Figure B.7: Dimensional details of the artwork representing the metalization pattern on an individual quartz circuit used in the 80/240 GHz frequency tripler (version 2).

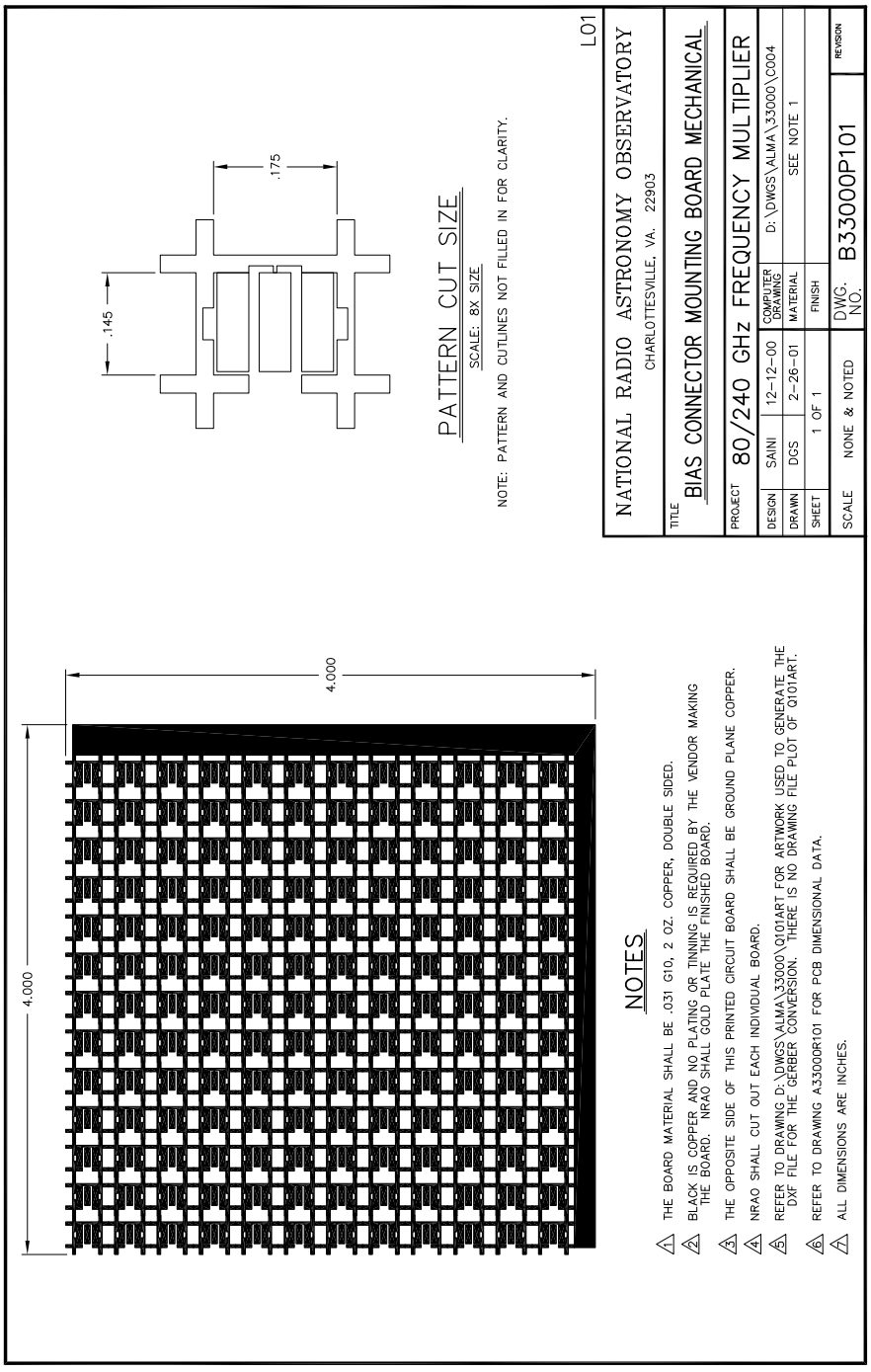


Figure B.8: Details of the artwork film used in the fabrication of printed circuit board for the DC bias circuit in the 80/240 GHz frequency tripler.

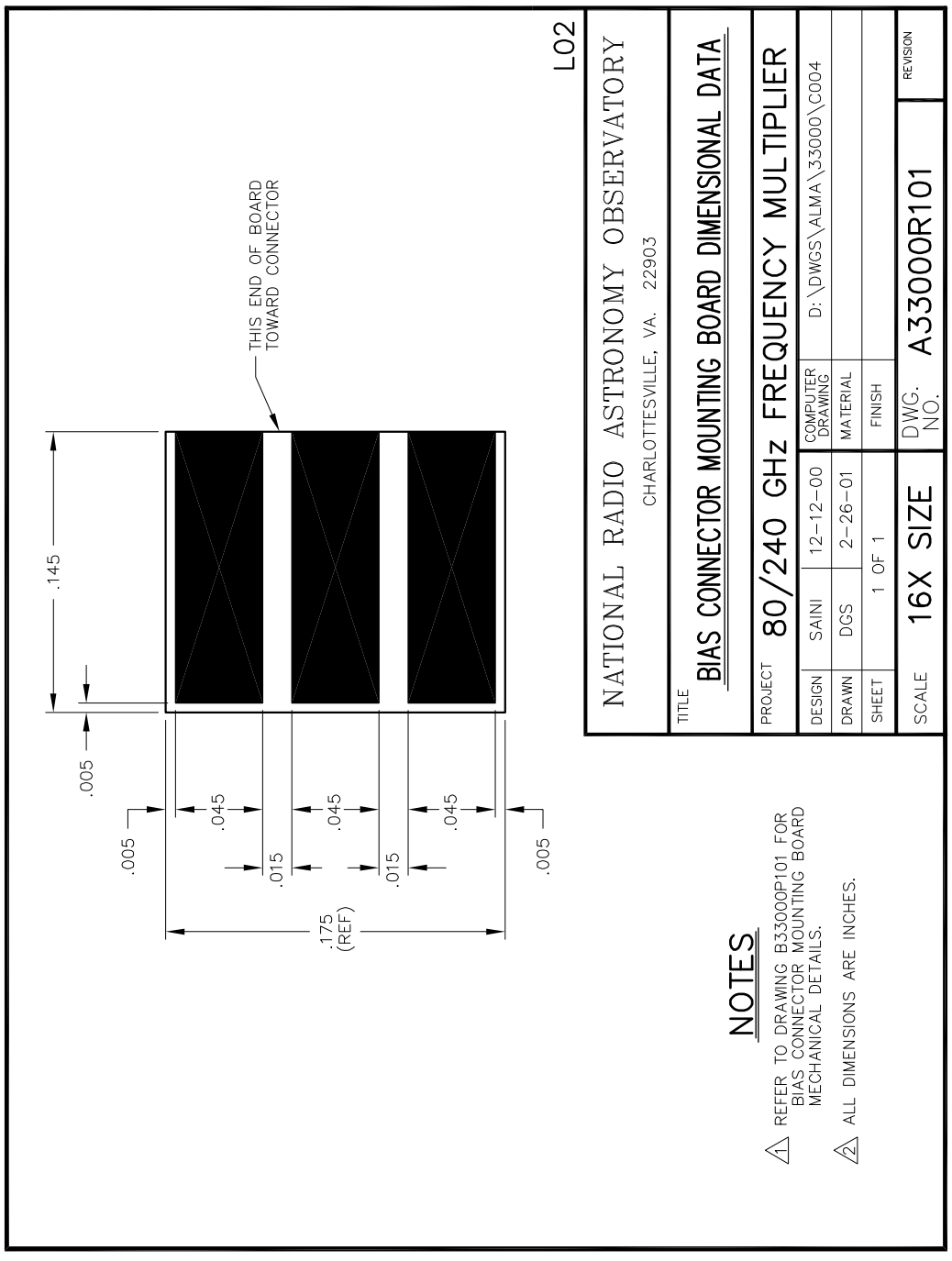


Figure B.9: Dimensional details of the artwork representing the metalization pattern on an individual DC bias board used in the 80/240 GHz frequency tripler.

Appendix C

Fabrication of Quartz Circuits

The technique for the fabrication of planar quartz circuits for various frequency multipliers is described in this appendix.

C.1 Circuit Fabrication for the 55/110 GHz Frequency Doubler

The linear embedding circuit for the 55/110 GHz frequency doubler consisted of a planar circuit housed in a metal waveguide block. The circuit was a polished 5 mil thick fused-quartz substrate with circuit metalization on one side. Fabrication of this circuit involved processing a 1 inch diameter circular

fused-quartz substrate to realize an array of circuits that were subsequently separated by dicing.

The fabrication process started by mounting the circular quartz substrate on a thick silicon wafer using G-wax. This was done to mechanically support the thin and fragile quartz substrate. The wafer was then cleaned with Ethanol, Tetrachloroethane, and Methanol on a spin cleaner. A 50 Å thick chromium seed layer was then sputtered on the quartz surface followed by a 500–1000 Å thick gold seed layer. Gold has poor adhesion with quartz and was therefore not deposited directly atop the quartz substrate. The chromium seed layer served to provide good adhesion to the quartz substrate, but its conductivity being much lower than that of gold, its thickness had to be kept very small to minimize circuit losses.

A 3.3 μm thick photo-resist layer was spun on top of the seed gold surface. The wafer was subsequently exposed to UV light through the photo-mask and developed. A 2.5 μm thick gold layer was then electro-plated on top of the exposed seed layer of gold. The photo-resist was then stripped off and the wafer subjected to a gold etch solution to remove the un-plated seed gold layer and electrically separate the circuits. Finally, the exposed chromium seed layer was etched away and the circuits were diced and separated.

A detailed recipe of the process is given below:

1. **Mounting the quartz substrate on to a silicon wafer**

   (a) Scribe a Si-wafer into a square slightly larger than the quartz substrate.

   (b) Place the Si-wafer on the hot plate at approximately 180^oC.

   (c) Coat the Si-wafer with G-wax.

(d) Place the quartz substrate on the Si-wafer.

(e) Remove any excess G-wax with acetone while still hot (do so quickly to avoid removing G-wax from under edges of quartz).

2. **Seed-metal deposition**

(a) Sputter about 50 Å thick Cr followed by 500–1000 Å thick Au on top of the quartz substrate.

3. **Photolithography**

(a) Spin-clean the quartz substrate mounted on the Si-wafer with Ethanol, Tetracholoroethane, and Methanol (rub with a damp swab while spinning to remove any dust particles).

(b) Expose to O_2 plasma for 10–20 minutes.

(c) Hot-plate bake at 120^oC for 3 minutes.

(d) Expose to HMDS vapors for 10 minutes.

(e) Spin AZ P4330 at 4000 RPM for 30 seconds. (This yields a 3.3 μm thick photo-resist layer. Do not use photo-resist that has been in the dropper bottle longer than a month.)

(f) Wait for 10 minutes, then hot-plate bake at 100^oC for 1 minute.

(g) UV expose for 30 seconds through photo-mask (with a UV intensity of 10 mW/cm^2). Both standard and HB exposure mode work well, but the HB mode is preferred. The standard mode blows nitrogen from bottom of substrate while the HB mode evacuates air between the mask and substrate resulting in better accuracy, especially when the feature sizes are small.

(h) Expose hole for mouse-trap using light microscope. Expose for 80 seconds using 10× lens with the aperture size reduced appropriately.

(i) Develop using AZ400K:DI-water (1:4) solution for 60–90 seconds, stopping when the developing process appears to be complete. Then rinse in DI-water for 1 minute.

(j) UV cure for 30 minutes, then oven bake at 120^oC for 20 minutes.

(k) Measure resist thickness on the Tencor and circuit feature sizes under an optical measuring microscope.

(l) Clean the exposure mask in AZ300T for 10–15 minutes, rinse in DI-water for 5–10 minutes, then oven bake at 120^oC for 15 minutes.

4. **Gold Electroplating**

(a) Mount the Si-wafer carrying the quartz substrate on a glass slide using G-wax.

(b) Clean by dipping in HCL:DI-water (1:2) solution for 3 minutes, then rinse in DI-water for 3 minutes.

(c) Expose to O_2 plasma for 5–10 minutes.

(d) Clean by dipping in HCL:DI-water (1:2) solution for 3 minutes, then rinse in DI-water for 3 minutes.

(e) Mount the slide on the mouse-trap.

(f) DC plate in Techni-Gold solution at 50^oC ($32\ pA/\mu m^2$). For a 2.25 μm plating thickness, this works out to 6.25 mA for 8 minutes and 30 seconds.

(g) Measure gold fill depth on the Tencor and perform additional plating if required.

(h) Remove wafer from mouse-trap, then clean mouse-trap with DI-water.

5. **Final Etch**

(a) Clean in heated AZ300T to remove photo-resist (heat to 80^oC, which is about 2 on the dial).

(b) Gold wet etch – Dip in Howard's Au etch HG400 for 45 seconds at room temperature. Continue etching till the seed-layer gold is evenly removed everywhere. Eching rate is 2000 Å/minute. Then rinse in DI-water.

(c) Dip in TFE chromium etch (1:1 with DI-water) solution for 1 minute at 30^oC, then rinse in DI-water.

(d) Measure the gold thickness on the Tencor and the circuit feature sizes under an optical measuring microscope.

6. **Dice and Separate**

C.2 Circuit Fabrication for the 110/220 GHz Frequency Doubler

The linear embedding circuit for the 110/220 GHz frequency doubler consisted of a planar circuit housed in a metal waveguide block. The circuit was a polished 2 mil thick fused-quartz substrate with circuit metalization on one

side. Fabrication of this circuit involved processing a 1 inch diameter circular fused-quartz substrate to realize an array of circuits that were subsequently separated by dicing.

The fabrication process started by mounting the circular quartz substrate on a thick silicon wafer using G-wax. This was done to mechanically support the thin and fragile quartz substrate. The wafer was then cleaned with Ethanol, Tetrachloroethane, and Methanol on a spin cleaner. A 50 Å thick chromium seed layer was then sputtered on the quartz surface followed by a 500–1000 Å thick gold seed layer. Gold has poor adhesion with quartz and was therefore not deposited directly atop the quartz substrate. The chromium seed layer served to provide good adhesion to the quartz substrate, but its conductivity being much lower than that of gold, its thickness had to be kept very small to minimize circuit losses.

A 3.3 μm thick photo-resist layer was spun on top of the seed gold surface. The wafer was subsequently exposed to UV light through the photo-mask and developed. A 2.5 μm thick gold layer was then electro-plated on top of the exposed seed layer of gold. The photo-resist was then stripped off and the wafer subjected to a gold etch solution to remove the un-plated seed gold layer and electrically separate the circuits. Finally, the exposed chromium seed layer was etched away and the circuits were diced and separated.

The recipe used for the fabrication of this planar quartz circuit was identical to that used for the fabrication of quartz circuits for the 55/110 GHz frequency doubler (described in Section-C.1).

C.3 Circuit Fabrication for the 80/240 GHz Frequency Tripler

The linear embedding circuits for the 80/240 GHz frequency tripler consisted of planar input and output circuits (first iteration) and a single quartz circuit (second iteration) housed in a metal waveguide block. These circuits were polished 1 mil thick fused-quartz substrates with circuit metalization on one side. Fabrication of these circuits involved processing a 1 inch diameter circular fused-quartz substrate to realize an array of circuits that were subsequently separated by dicing.

The fabrication process started by mounting the circular quartz substrate on a thick silicon wafer using black wax. This was done to mechanically support the thin and fragile quartz substrate. The wafer was then cleaned with Ethanol and Methanol on a spin cleaner. A 100 Å thick titanium seed layer was then sputtered on the quartz surface followed by a 1000 Å thick gold seed layer. Gold has poor adhesion with quartz and was therefore not deposited directly atop the quartz substrate. The titanium seed layer served to provide good adhesion to the quartz substrate, but its conductivity being much lower than that of gold, its thickness had to be kept very small to minimize circuit losses.

A 2.8 μm thick photo-resist layer was spun on top of the seed gold surface. The wafer was subsequently exposed to UV light through the photo-mask and developed. A 1.6 μm thick gold layer was then electro-plated on top of the exposed seed layer of gold. The photo-resist was then stripped off and the wafer subjected to a gold etch solution to remove the un-plated seed gold

layer and electrically separate the circuits. Finally, the exposed titanium seed layer was etched away and the circuits were diced and separated.

A detailed recipe of the process is given below:

1. **Mounting the quartz substrate on to a silicon wafer**

   (a) Scribe a Si-wafer into a square slightly larger than the quartz substrate.

   (b) Spin-clean the Si-wafer with Ethanol, Tetrachloroethane, and Methanol (rub with damp swap while spinning to remove any debris or particles), then blow dry.

   (c) Dropper four drops of black wax dissolved in Tetrachloroethane on the Si-wafer.

   (d) Bake at 105^oC for 10 minutes in an oven. If "crater" formation is observed, add one drop of Tetracholoroethane on the black wax and allow time for it to dissolve.

   (e) Hot-plate bake at 100^oC for 5 minutes, then at 120^oC for 5 minutes, and finally at 130^oC for 5 minutes or until all the bubbles boil off.

   (f) Place the 1 mil thick quartz substrate on the black wax.

   (g) Hot-plate bake at 160^oC for 10 minutes.

   (h) If needed, blow nitrogen from top to gently force the quartz substrate to settle into the black wax.

   (i) Hot-plate bake again at 190^oC for about 5 minutes or until the black wax spreads to the edges of the wafer. Exercise care to avoid getting any wax on the top surface of the quartz.

2. **Seed-metal deposition**

   (a) Sputter about 100 Å Ti followed by 1000 Å thick Au on top of the quartz substrate.

3. **Photolithography**

   (a) Spin-clean the quartz substrate mounted on the Si-wafer with Ethanol and Methanol (rub with a damp swab while spinning to remove any dust particles).

   (b) Expose to O_2 plasma for 10–20 minutes.

   (c) Hot-plate bake at 120^oC for 3 minutes.

   (d) Expose to HMDS vapors for 10 minutes.

   (e) Spin AZ P4210 at 4000 RPM for 30 seconds. (This yields a 2.8 μm thick photo-resist layer. Do not use photo-resist that has been in the dropper bottle longer than a month.)

   (f) Wait for 10 minutes, then hot-plate bake at 100^oC for 1 minute.

   (g) UV expose for 45 seconds through photo-mask (with a UV intensity of 7 mW/cm^2). Both standard and HB exposure mode work well, but the HB mode is preferred. The standard mode blows nitrogen from bottom of substrate while the HB mode evacuates air between the mask and substrate resulting in better accuracy, especially when the feature sizes are small.

   (h) Expose hole for mouse-trap using light microscope. Expose for 80 seconds using 10× lens with the aperture size reduced appropriately.

(i) Develop using AZ400K:DI-water (1:4) solution for 2–4 minutes, stopping when the developing process appears to be complete. Then rinse in DI-water for 1 minute.

(j) UV cure for 20 minutes, then hot-plate bake at 100^oC for 1 minute. Next, transfer to a hot-plate at 120^oC and let stand for another minute.

(k) Measure resist thickness on the Tencor and circuit feature sizes under an optical measuring microscope.

(l) Clean the exposure mask in AZ300T for 10–15 minutes, rinse in DI-water for 5–10 minutes, then oven bake at 120^oC for 15 minutes.

4. **Gold Electroplating**

(a) Mount the Si-wafer carrying the quartz substrate on a glass slide using G-wax.

(b) Clean by dipping in HCL:DI-water (1:2) solution for 3 minutes, then rinse in DI-water for 3 minutes.

(c) Expose to O_2 plasma for 5–10 minutes.

(d) Clean by dipping in HCL:DI-water (1:2) solution for 3 minutes, then rinse in DI-water for 3 minutes.

(e) Mount the slide on the mouse-trap.

(f) DC plate in Techni-Gold solution at 50^oC (32 $pA/\mu m^2$). For a 1.6 μm plating thickness, this works out to 6.25 mA for 5 minutes.

(g) Measure gold fill depth on the Tencor and perform additional plating if required.

(h) Remove wafer from mouse-trap, then clean mouse-trap with DI-water.

5. **Final Etch**

(a) Clean in heated AZ300T to remove photo-resist (heat to 80^oC, which is about 2 on the dial).

(b) Gold wet etch – Dip in Howard's Au etch HG400 for 45 seconds at room temperature. Continue etching till the seed-layer gold is evenly removed everywhere. Eching rate is 2000 Å/minute. Then rinse in DI-water.

(c) Dip in Buffered Oxide Etchant (10:1 with DI-water) solution for 3 seconds at a time until all the Titanium is etched away. Then rinse thoroughly in DI-water to remove all traces of the oxide etchant.

(d) Measure the gold thickness on the Tencor and the circuit feature sizes under an optical measuring microscope.

6. **Dice and Separate**

Appendix D

Mechanical Drawings

The mechanical drawings of the frequency multiplier mounts are presented in this appendix. The drawings are ordered with the drawings corresponding to the 55/110 GHz frequency doubler placed first, followed by those corresponding to the 110/220 GHz frequency doubler. The drawings for the 80/240 GHz frequency tripler (versions 1 and 2) are placed at the end.

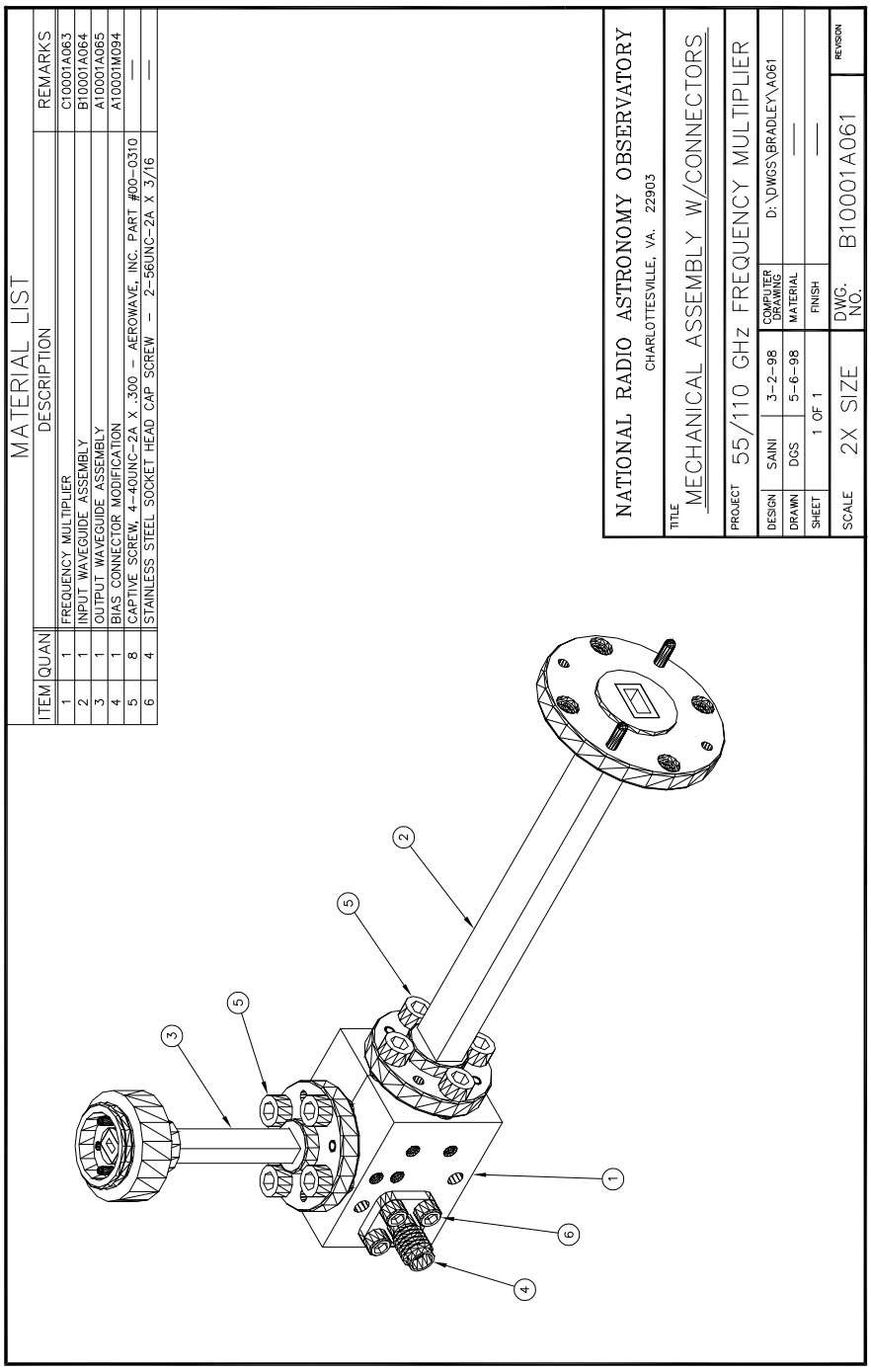


Figure D.1: 55/110 GHz frequency doubler: Mechanical assembly of the split block showing the DC bias connector and the waveguide flange adapters.

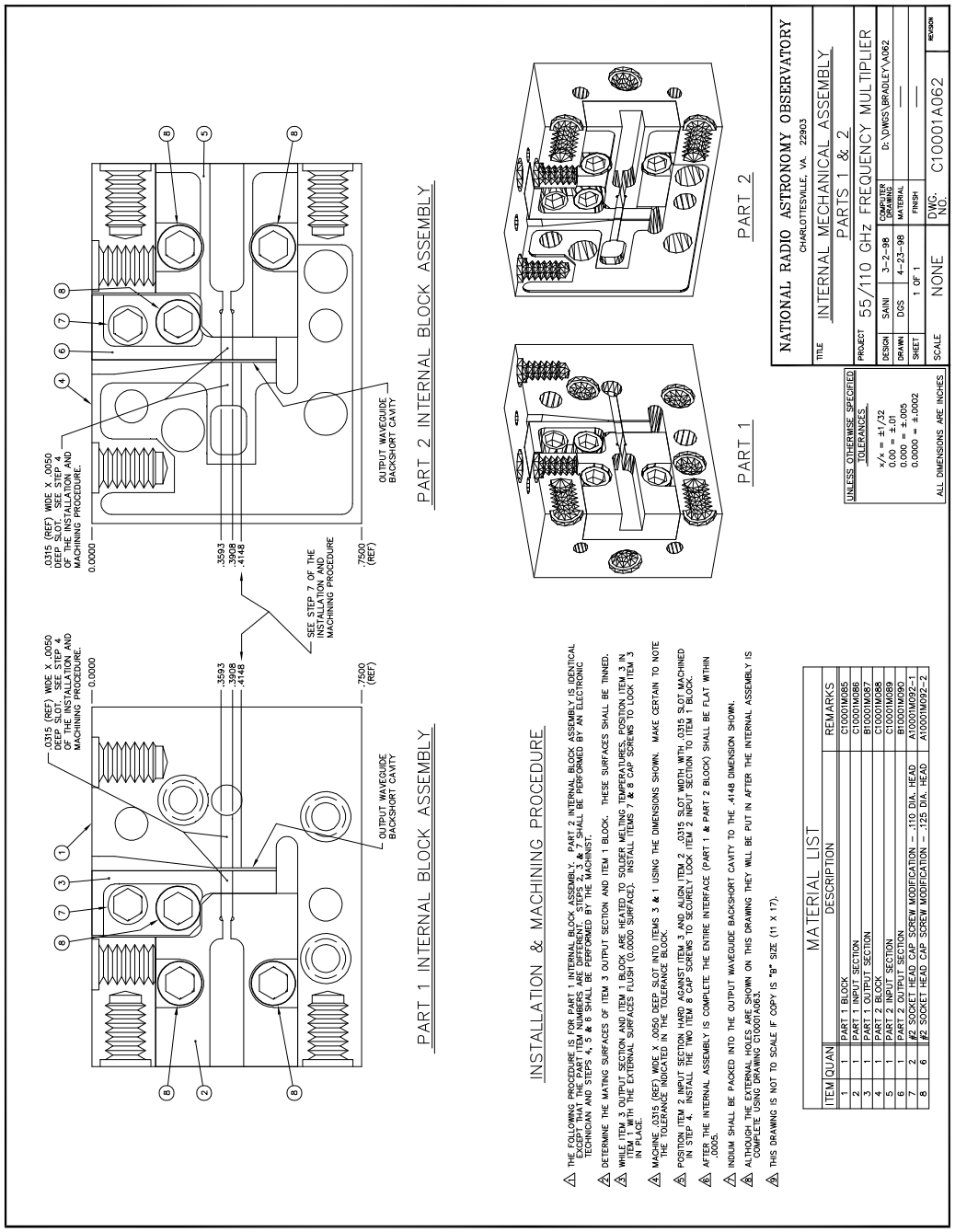


Figure D.2: 55/110 GHz frequency doubler: Internal mechanical assembly of parts 1 and 2 of the split block.

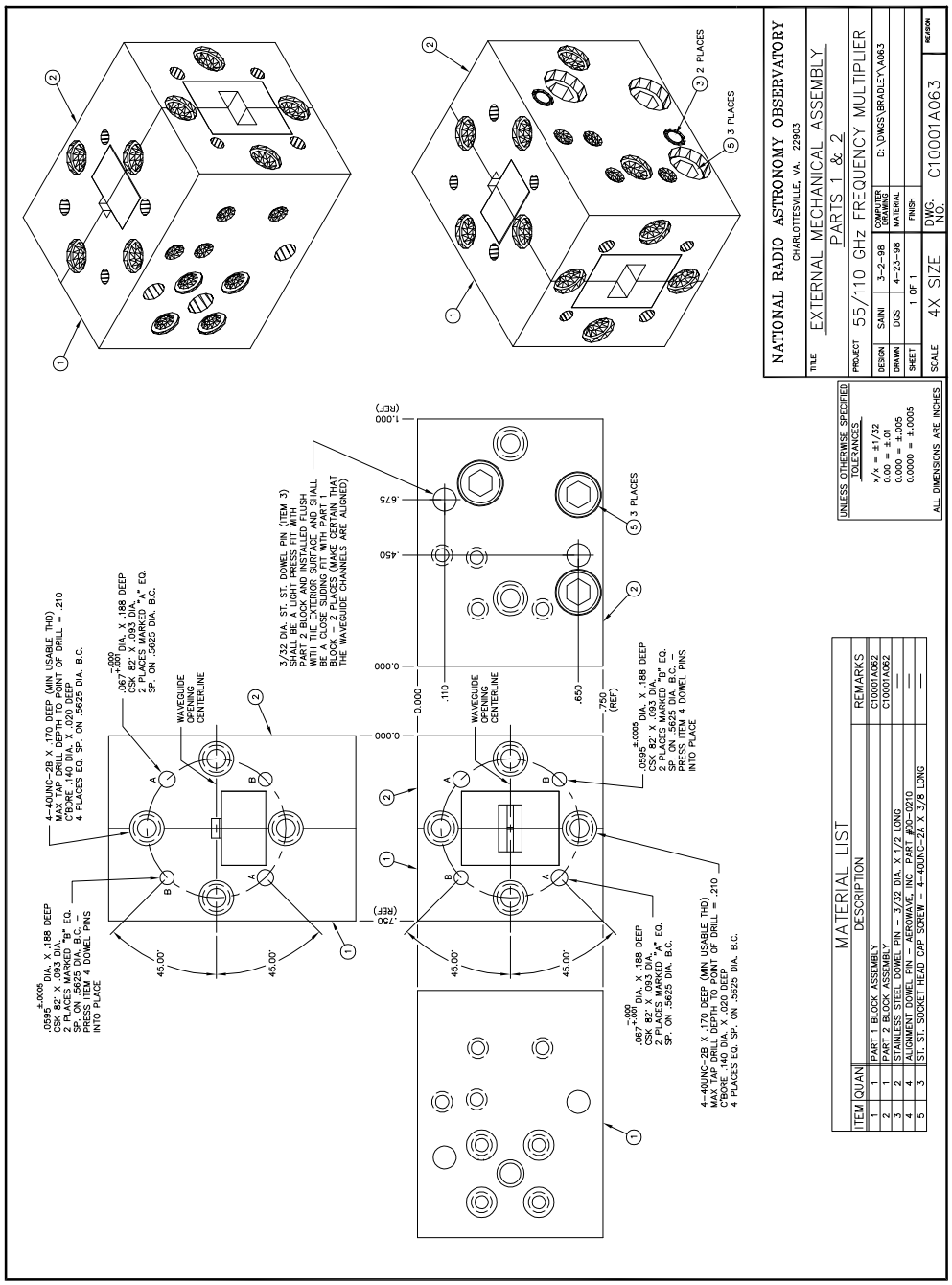


Figure D.3: 55/110 GHz frequency doubler: External mechanical assembly of parts 1 and 2 of the split block.

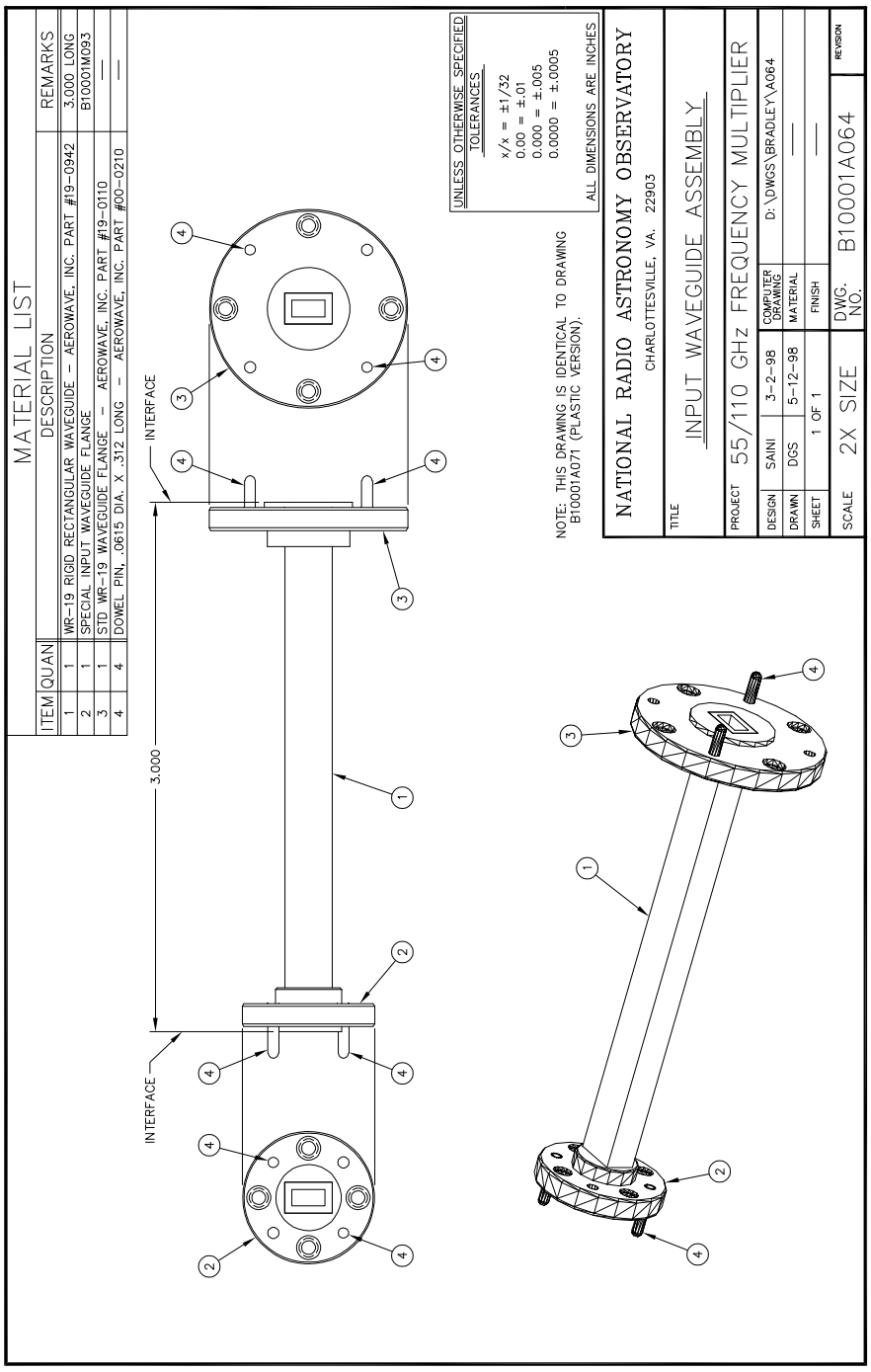


Figure D.4: 55/110 GHz frequency doubler: WR-19 input waveguide flange adapter assembly.

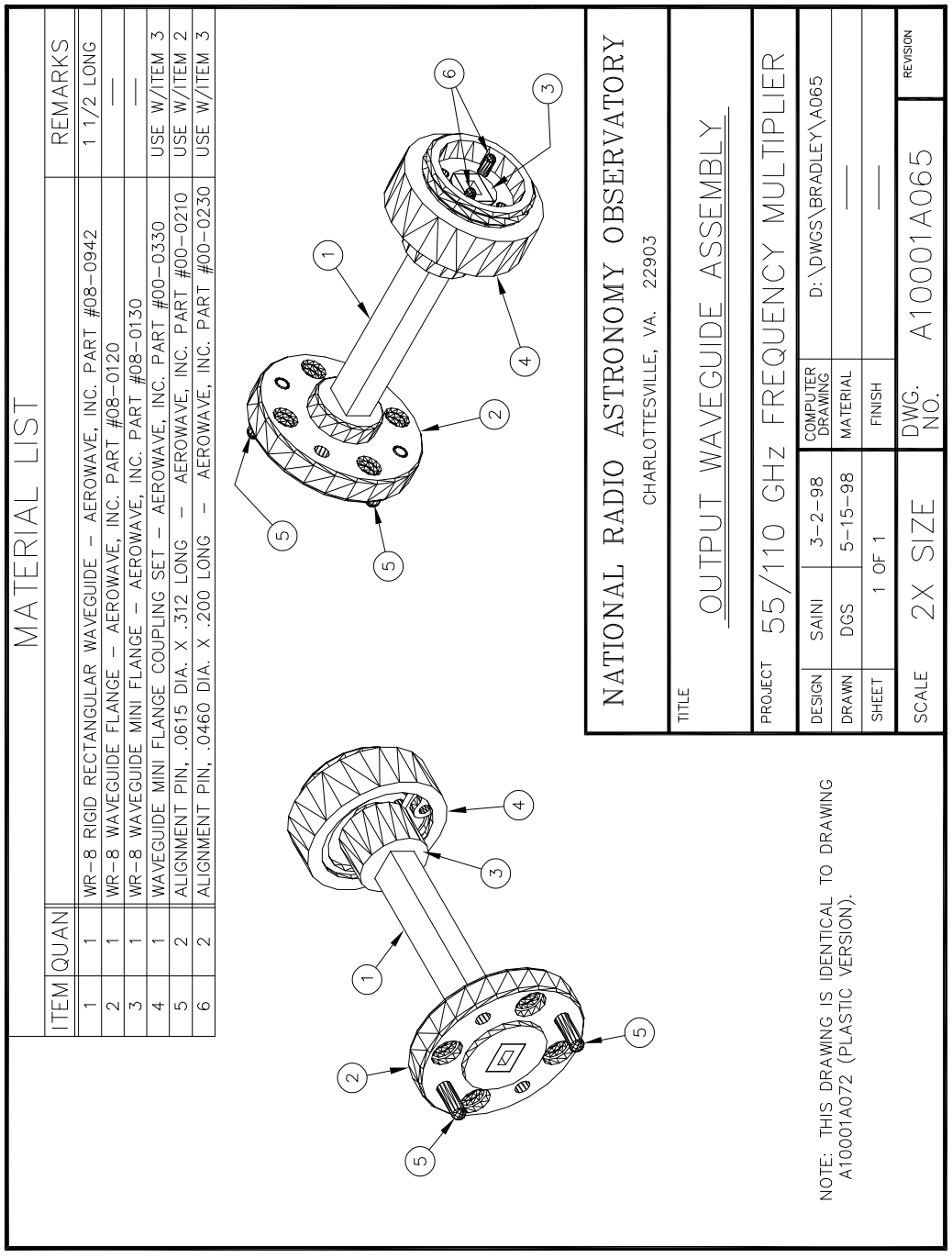


Figure D.5: 55/110 GHz frequency doubler: WR-8 output waveguide flange adapter assembly.

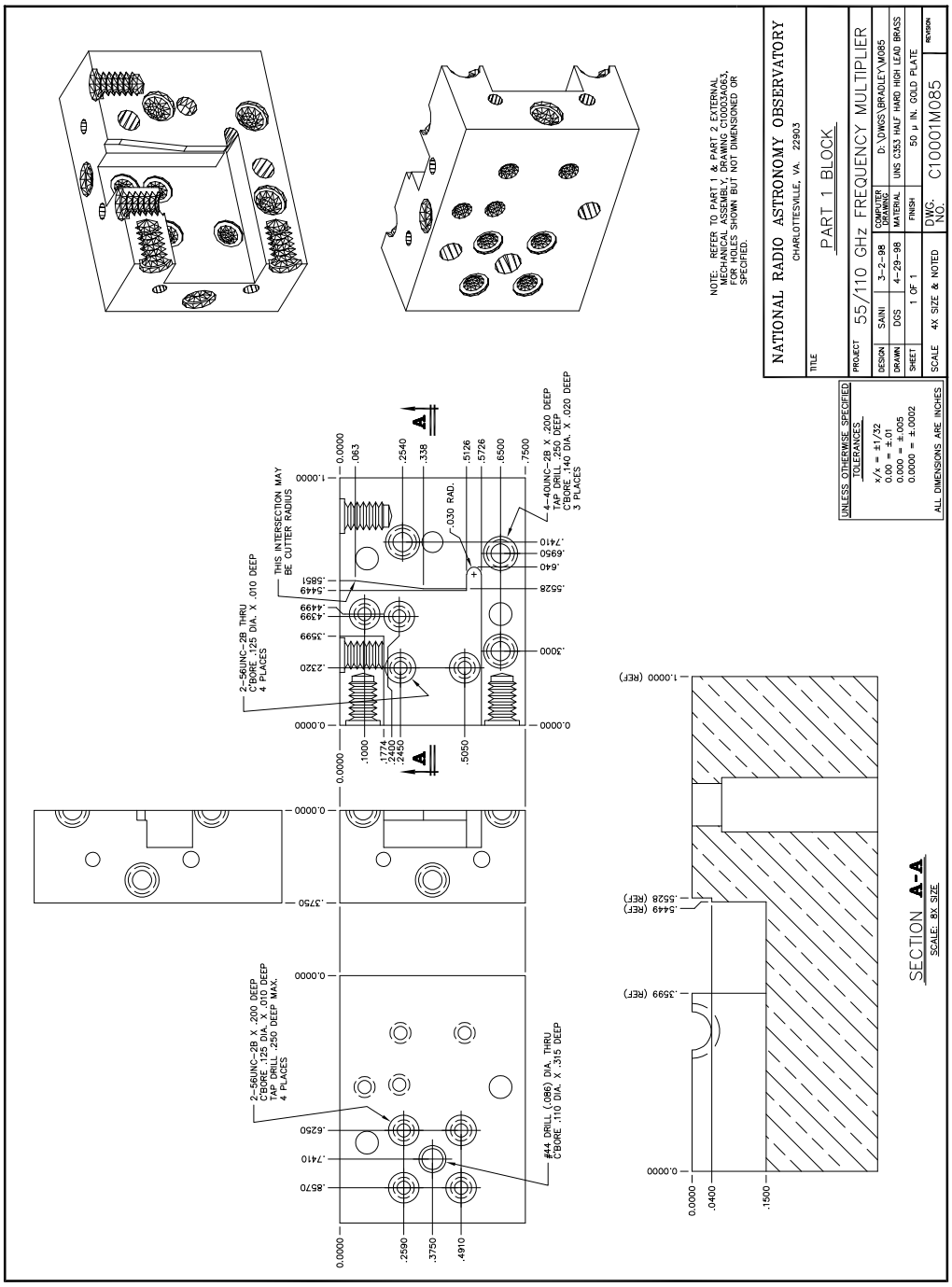


Figure D.6: 55/110 GHz frequency doubler: Mechanical details of part 1 of the two piece split block.

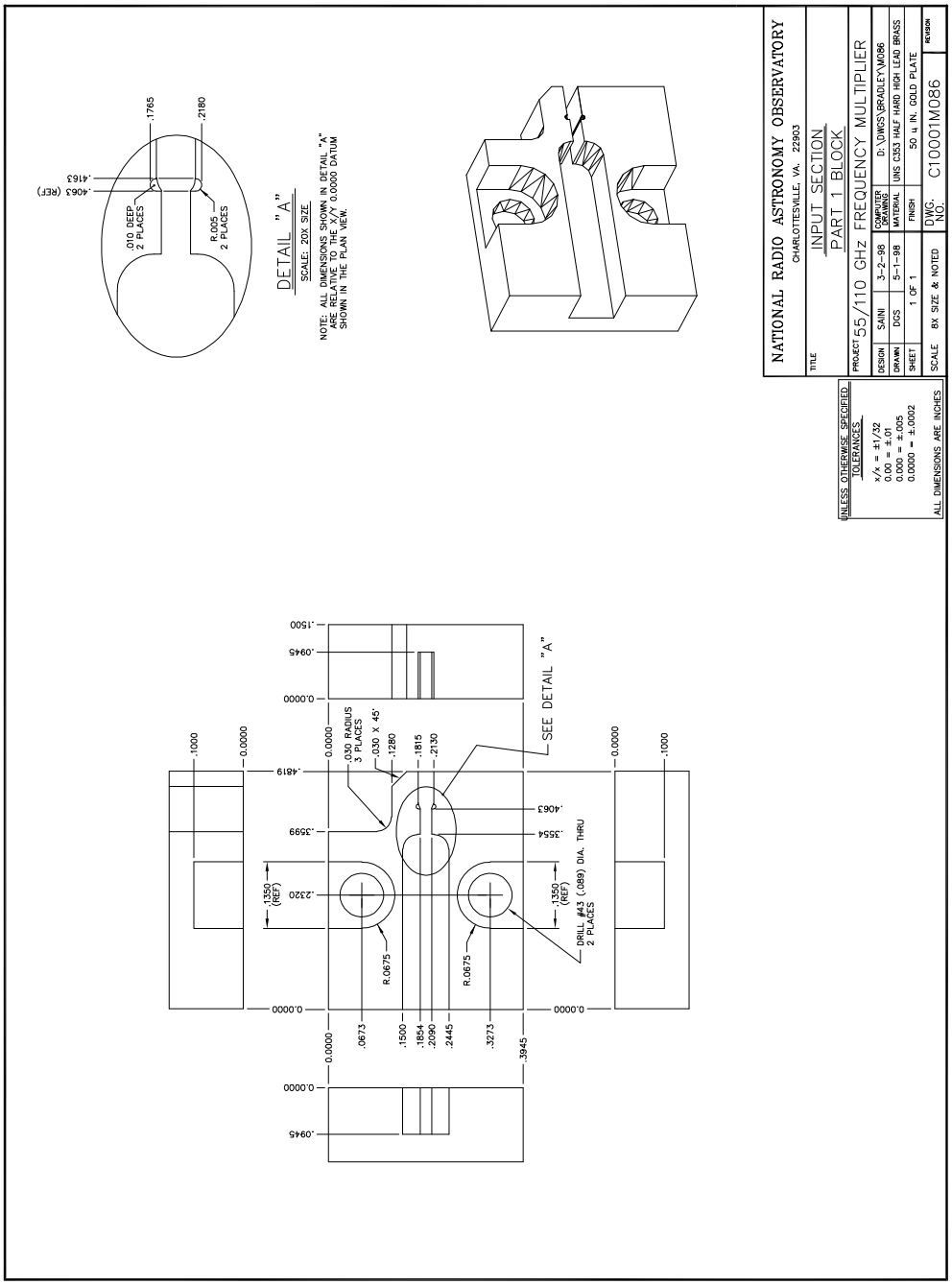


Figure D.7: 55/110 GHz frequency doubler: Mechanical details of the input section insert of part 1 of the two piece split block.

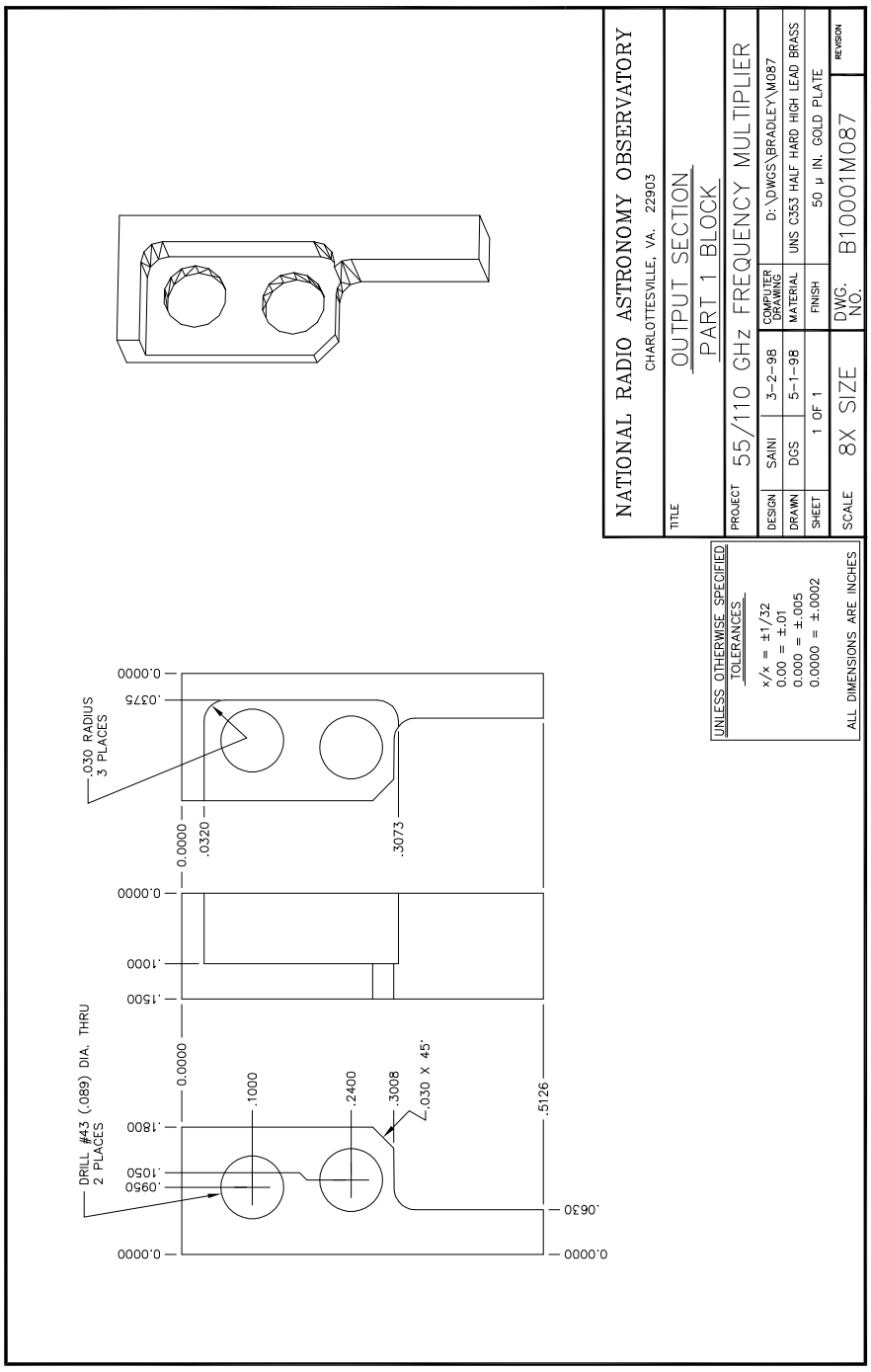


Figure D.8: 55/110 GHz frequency doubler: Mechanical details of the output section insert of part 1 of the two piece split block.

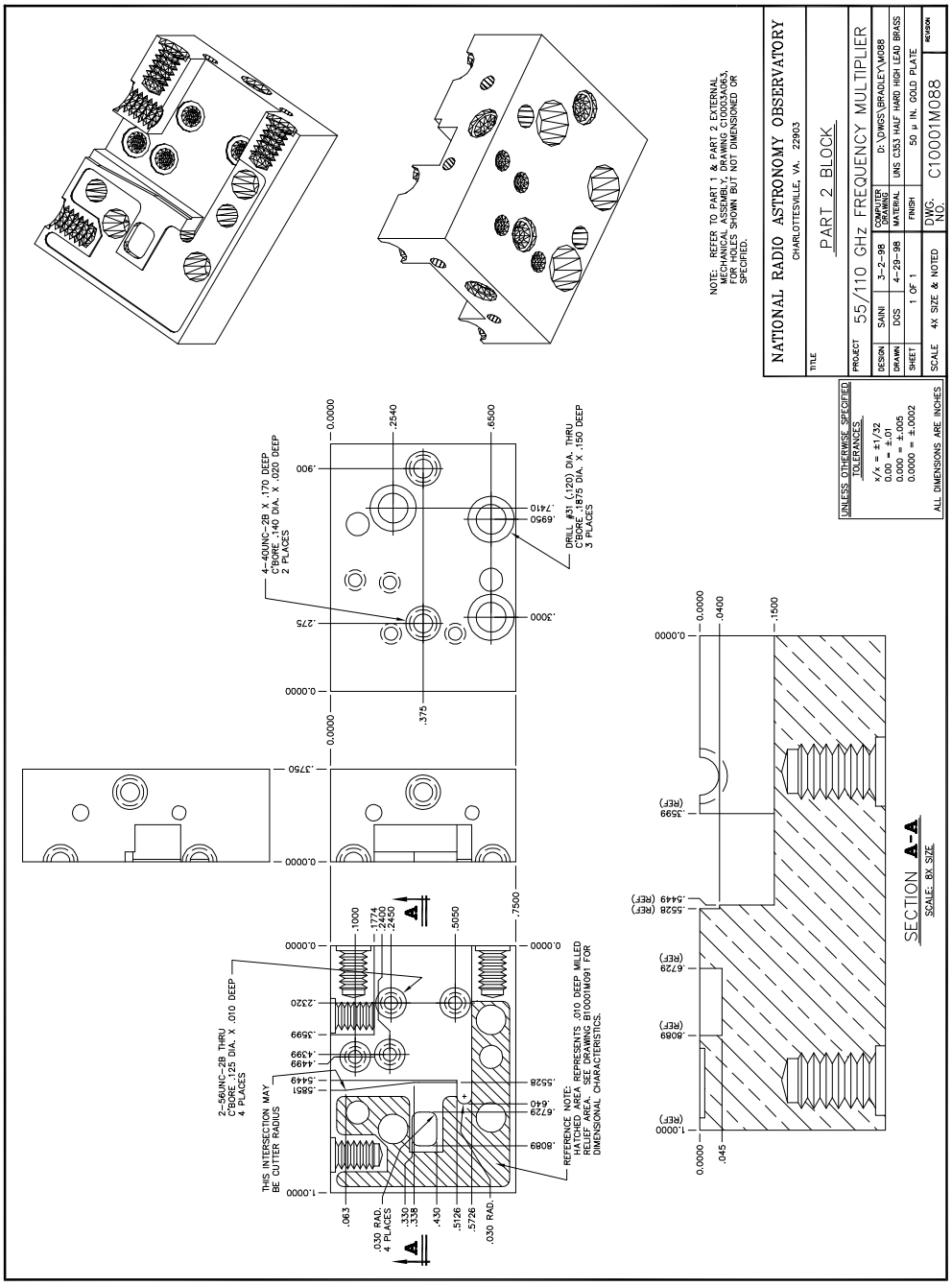


Figure D.9: 55/110 GHz frequency doubler: Mechanical details of part 2 of the two piece split block.

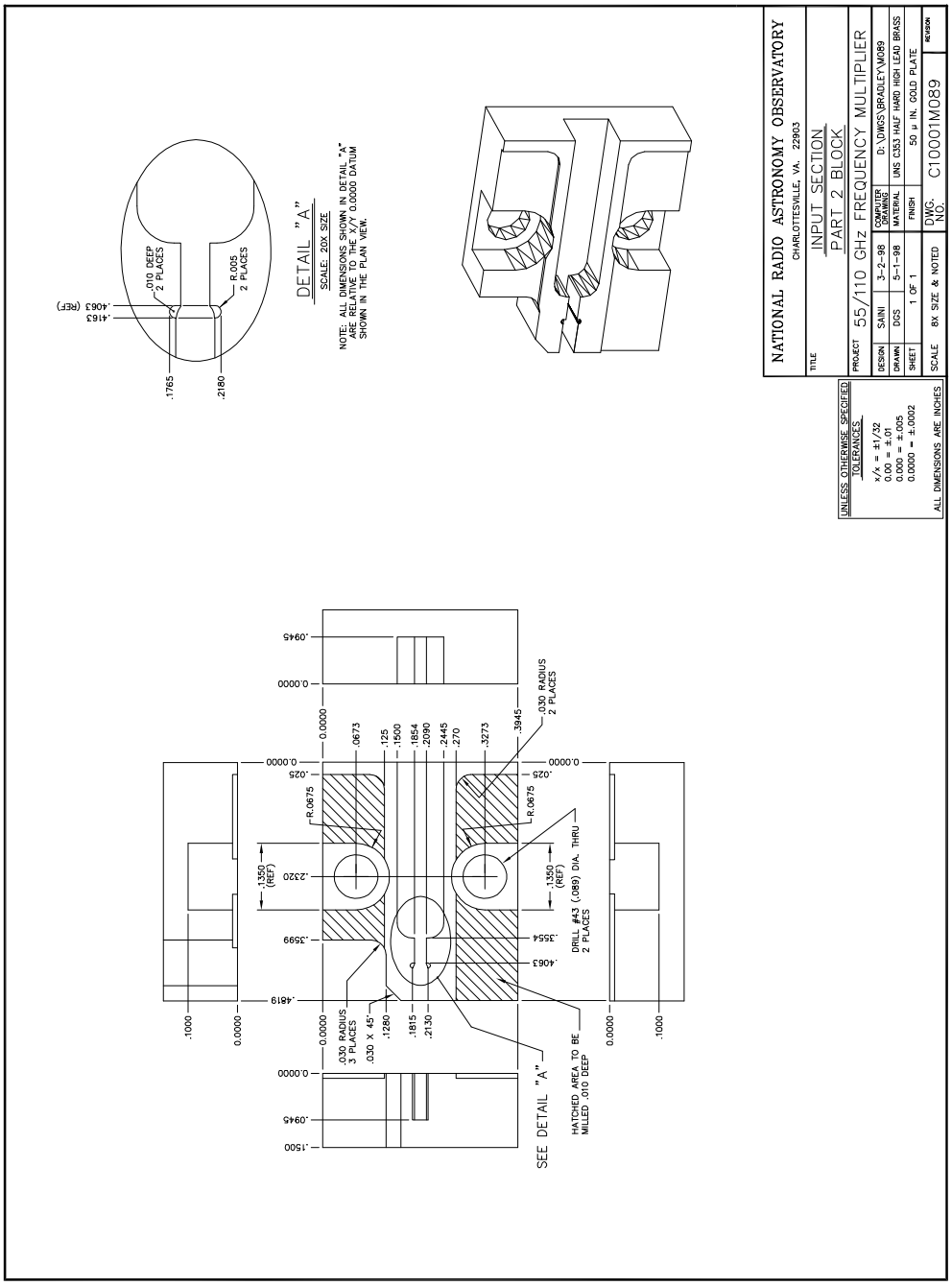


Figure D.10: 55/110 GHz frequency doubler: Mechanical details of the input section insert of part 2 of the two piece split block.

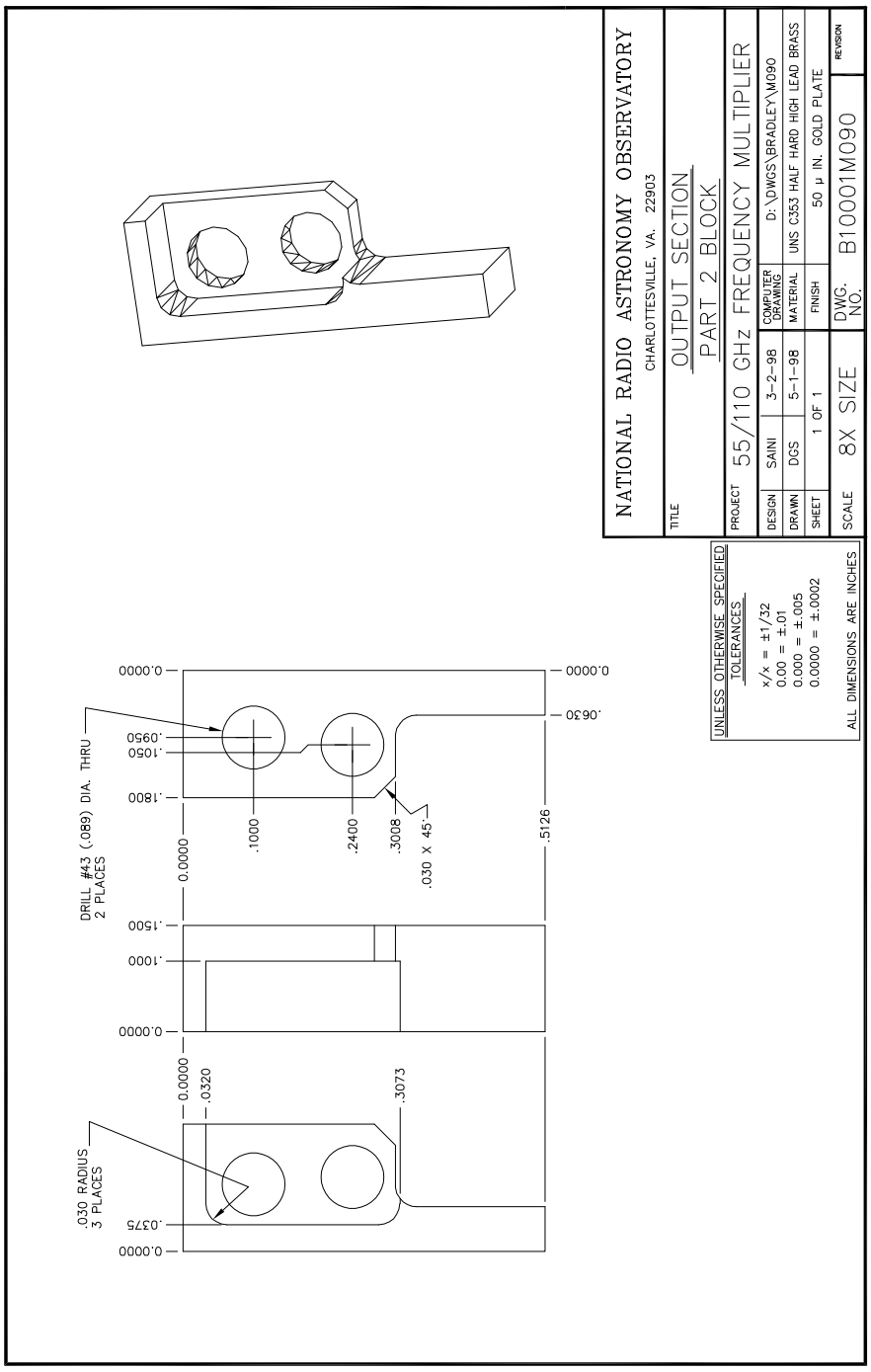


Figure D.11: 55/110 GHz frequency doubler: Mechanical details of the output section insert of part 2 of the two piece split block.

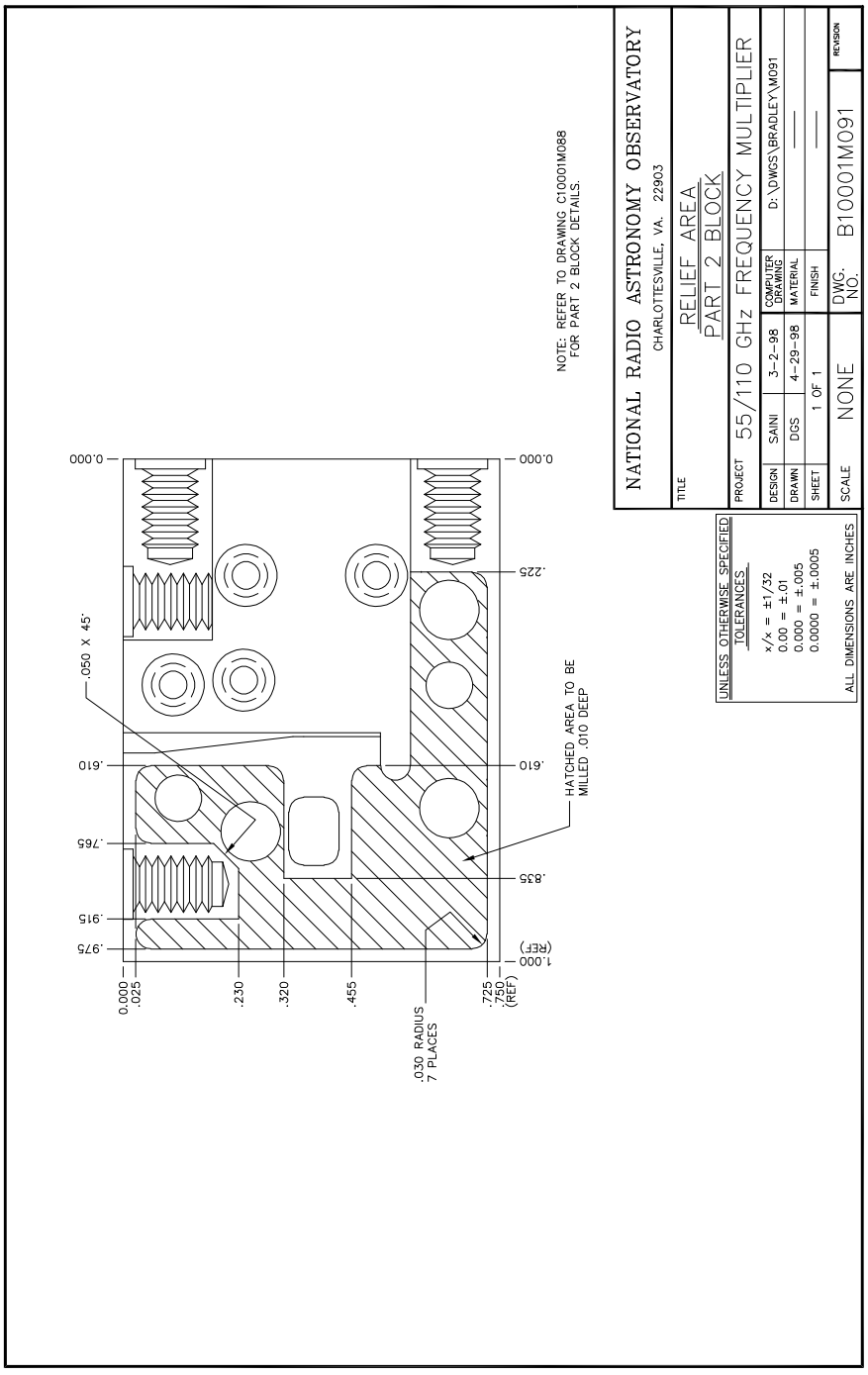


Figure D.12: 55/110 GHz frequency doubler: Location of the relief area in one of the halves (part 2) of the two piece split block.

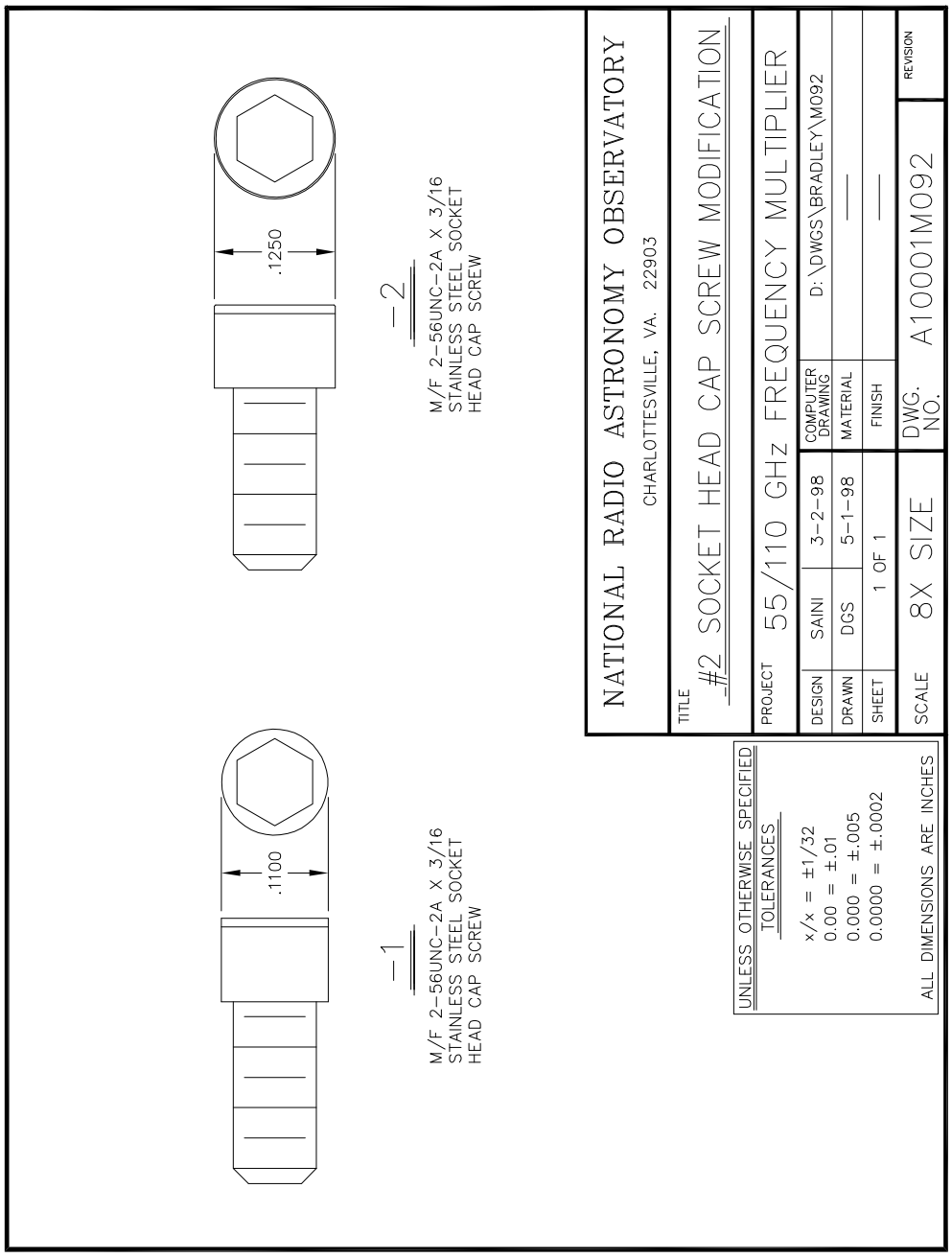


Figure D.13: 55/110 GHz frequency doubler: Details of the modified socket screws used to secure the input and output inserts into the two halves of the split block.

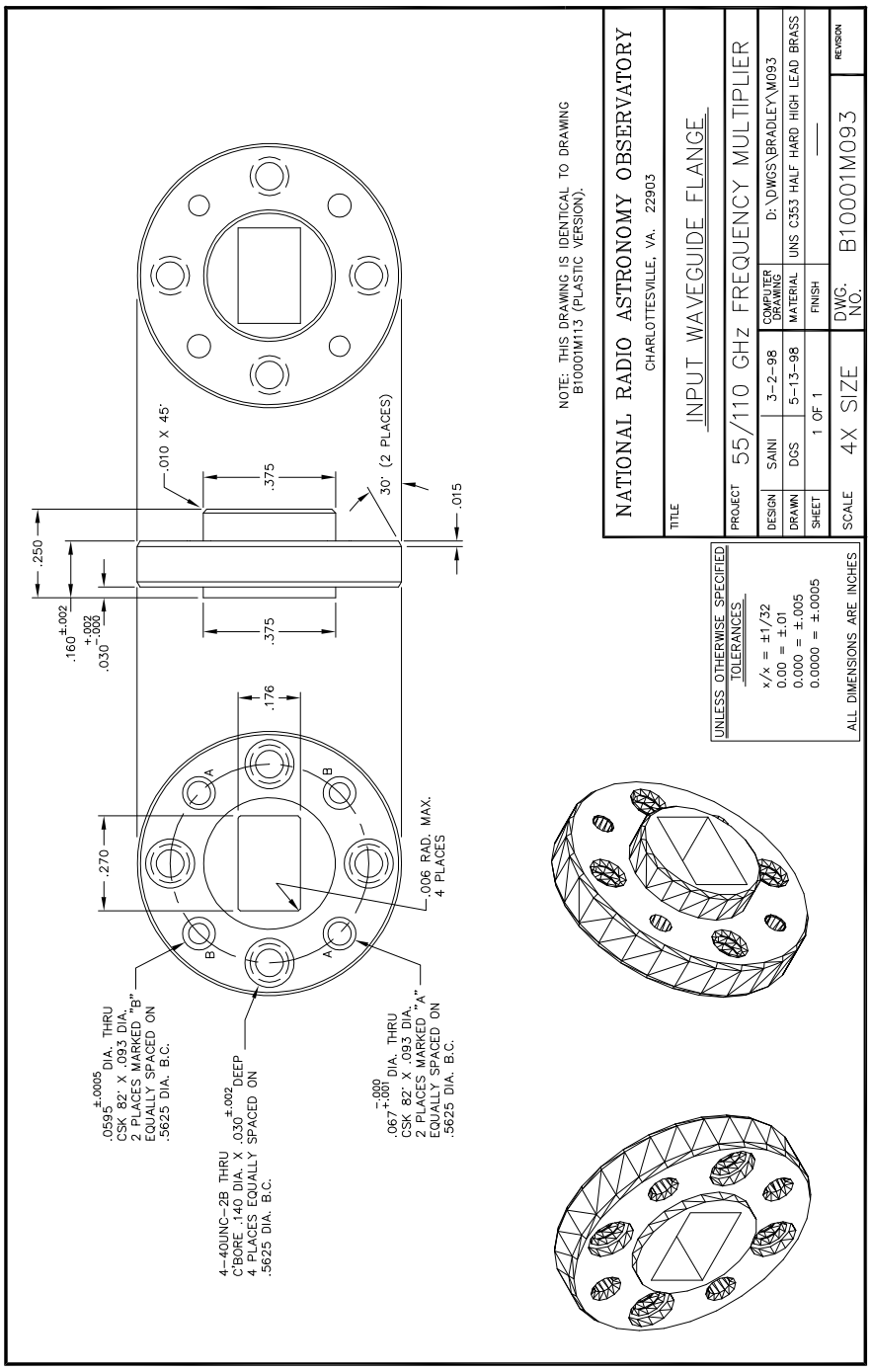


Figure D.14: 55/110 GHz frequency doubler: Mechanical details of the special WR-19 input waveguide flange.

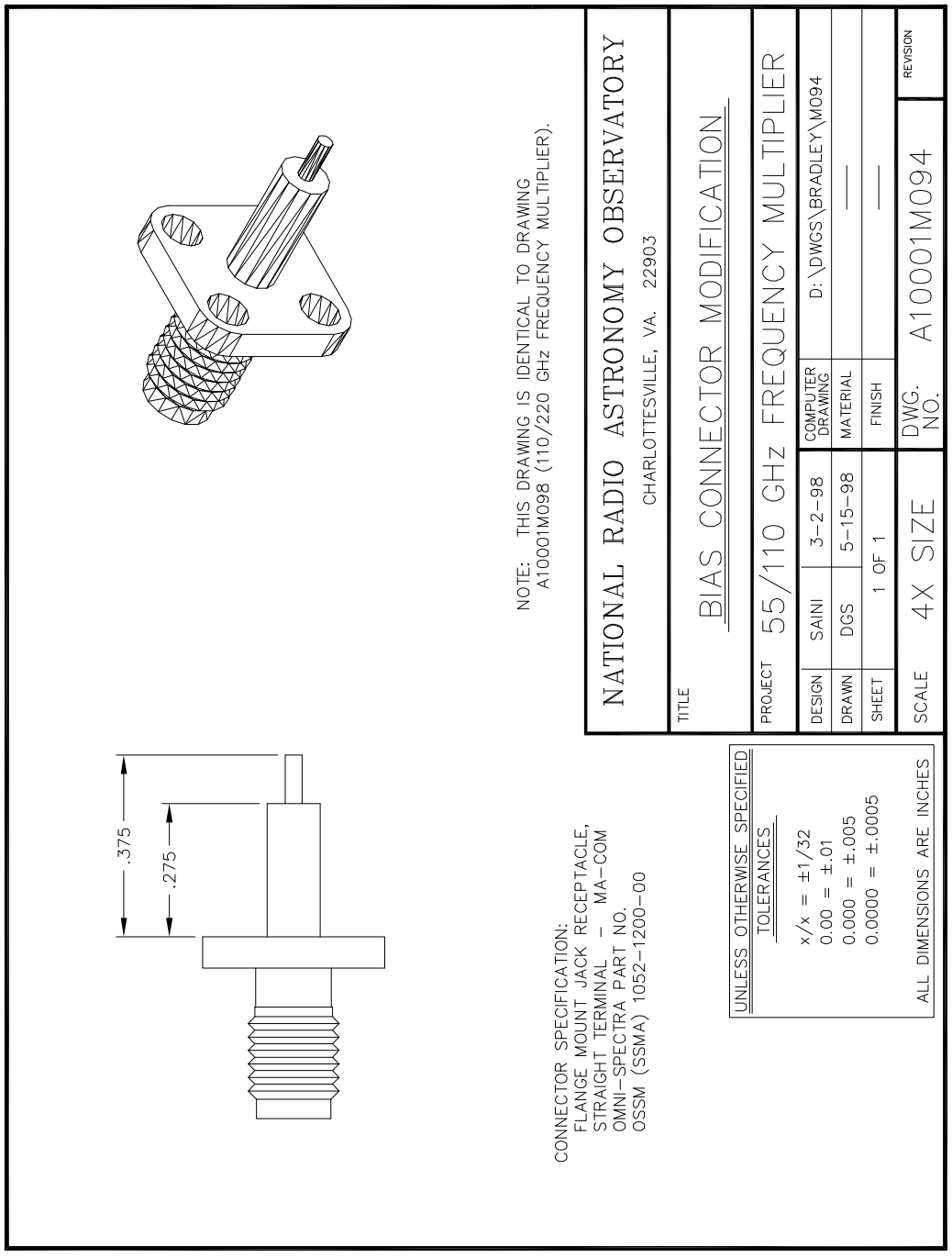


Figure D.15: 55/110 GHz frequency doubler: Details of the modified SSMA flange mount jack receptacle used as the DC bias connector.

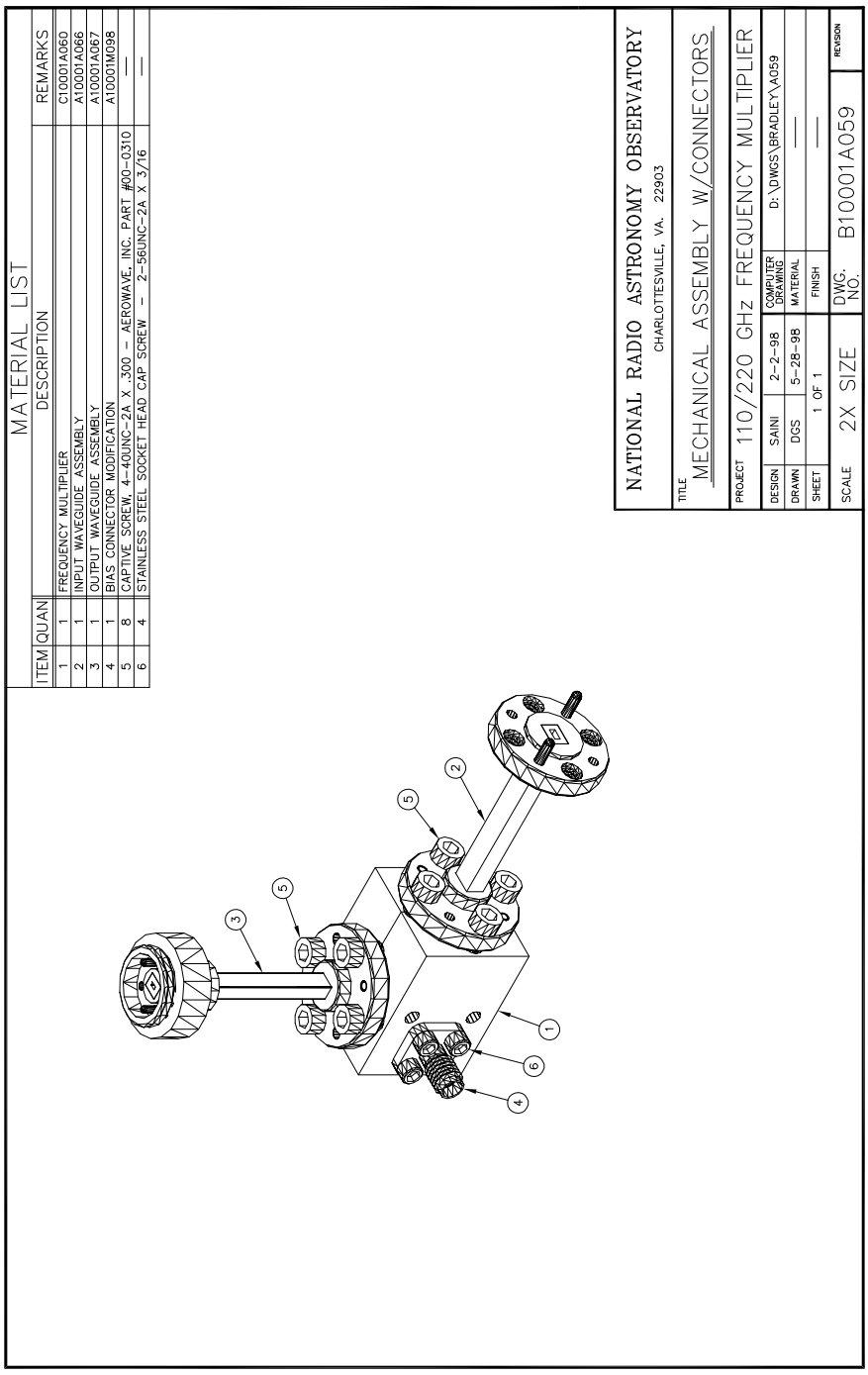


Figure D.16: 110/220 GHz frequency doubler: Mechanical assembly of the split block showing the DC bias connector and the waveguide flange adapters.

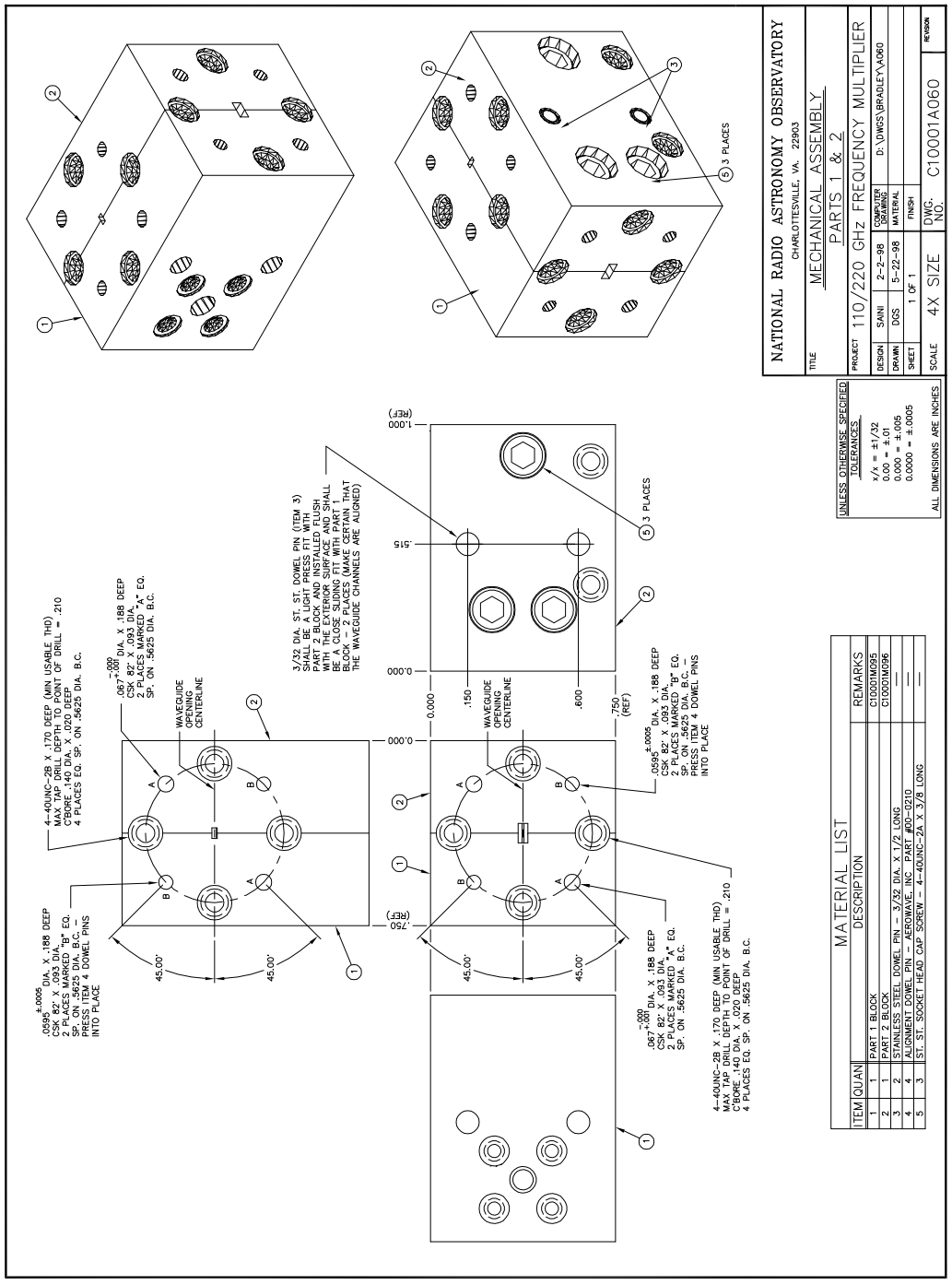


Figure D.17: 110/220 GHz frequency doubler: External mechanical assembly of parts 1 and 2 of the split block.

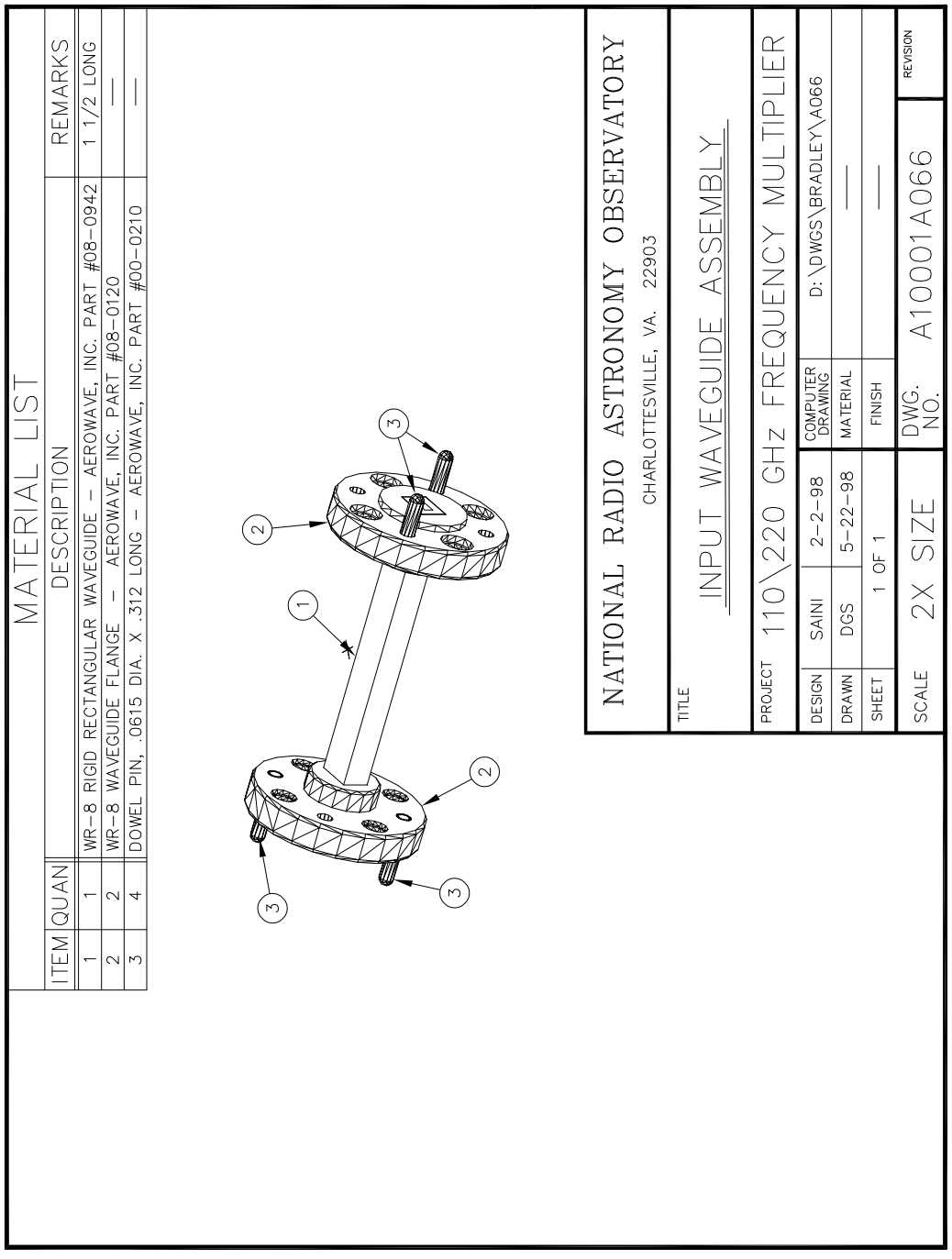


Figure D.18: 110/220 GHz frequency doubler: WR-8 input waveguide flange adapter assembly.

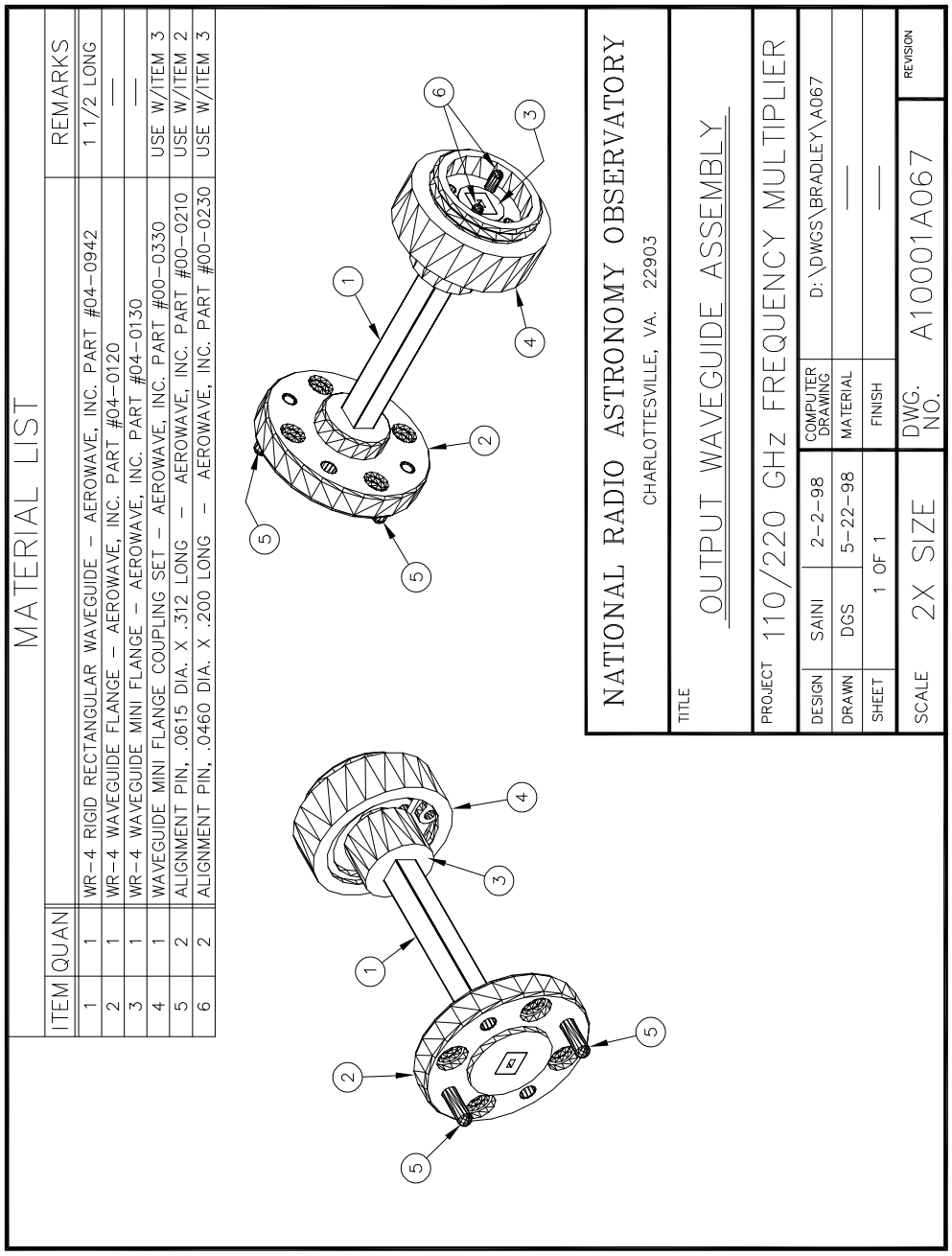


Figure D.19: 110/220 GHz frequency doubler: WR-4 output waveguide flange adapter assembly.

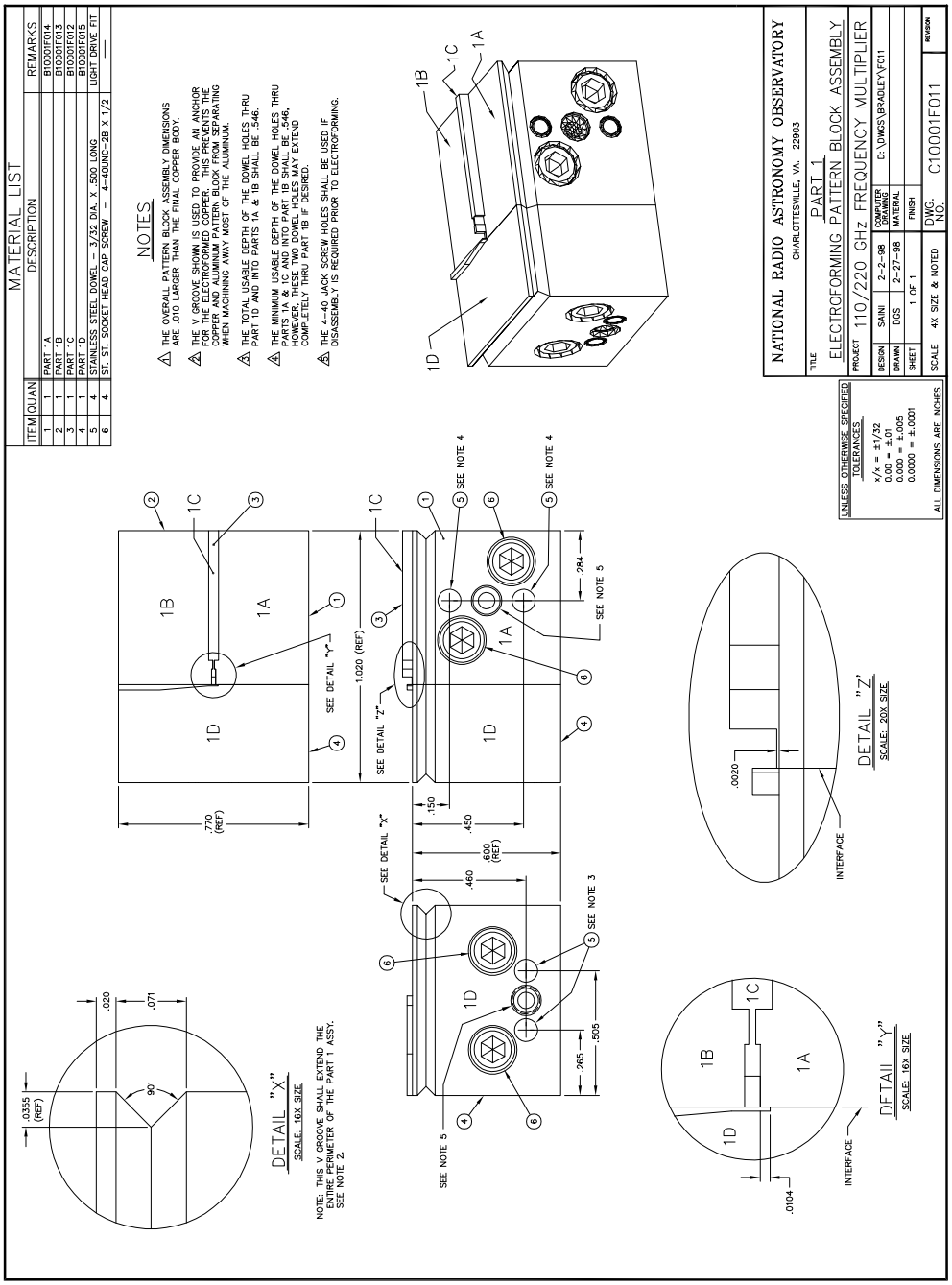


Figure D.20: 110/220 GHz frequency doubler: Assembly of the mandrel components 1A through 1D. This mandrel was used for electroforming part 1 of the split block.

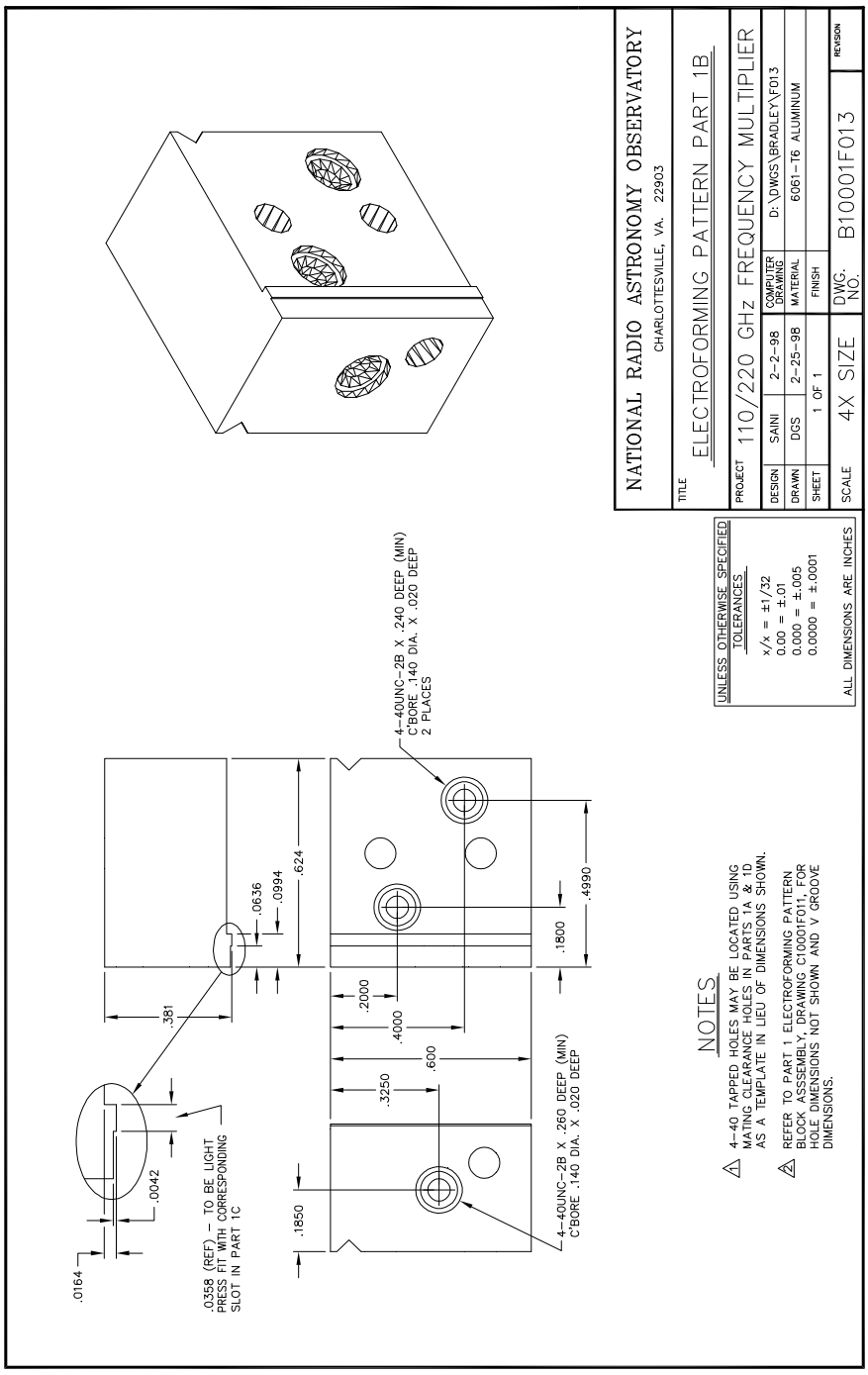


Figure D.21: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 1A.

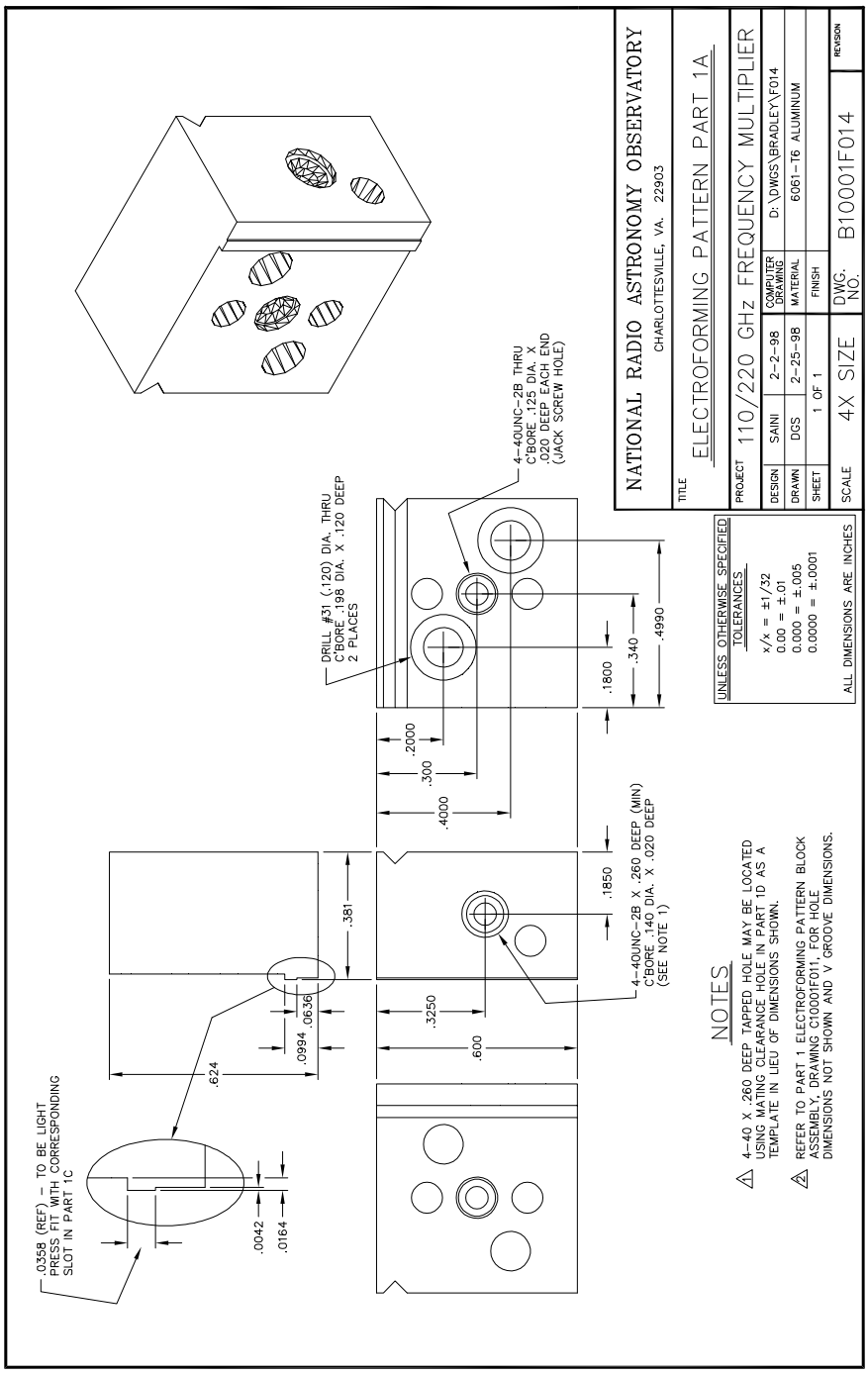


Figure D.22: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 1B.

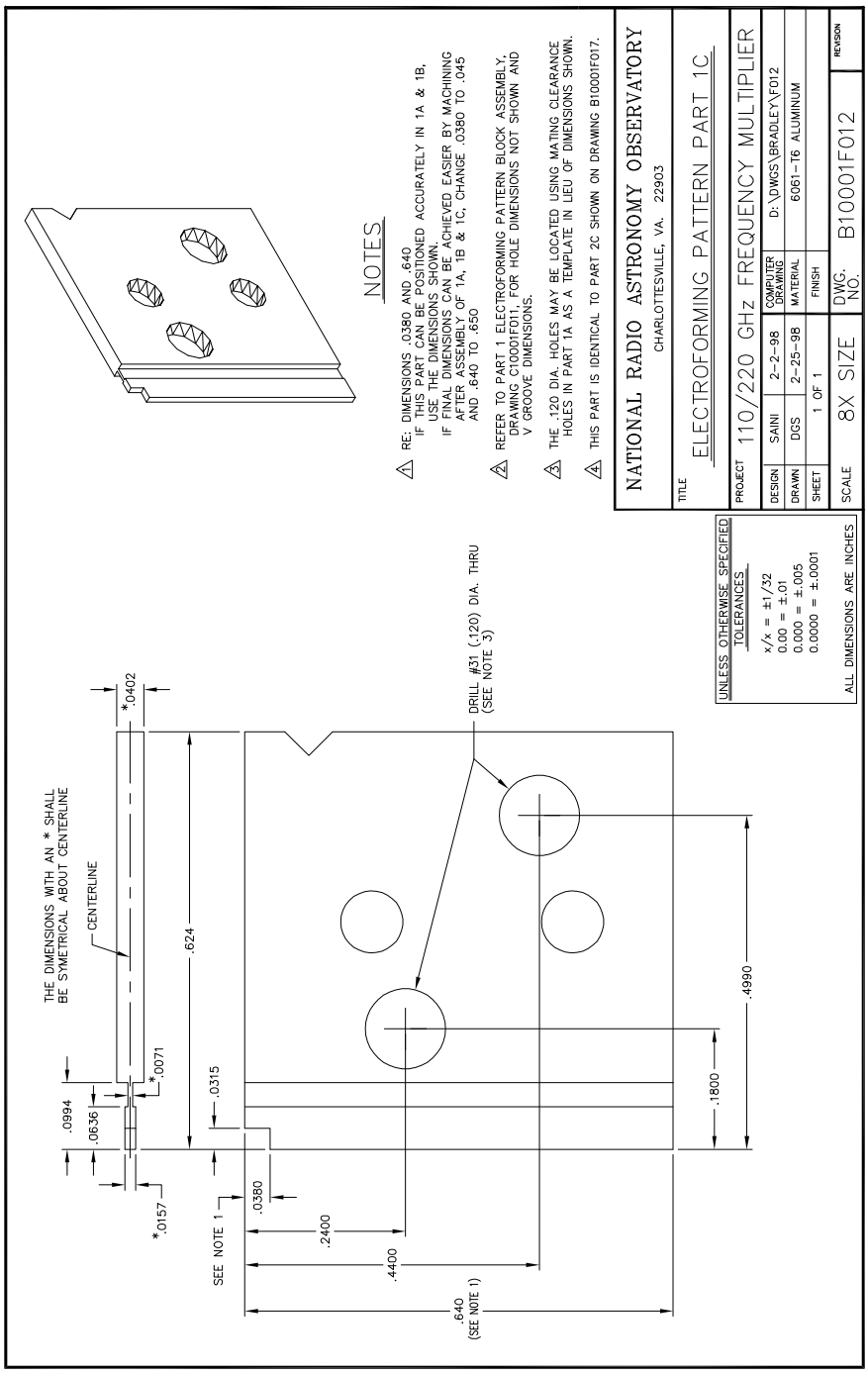


Figure D.23: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 1C.

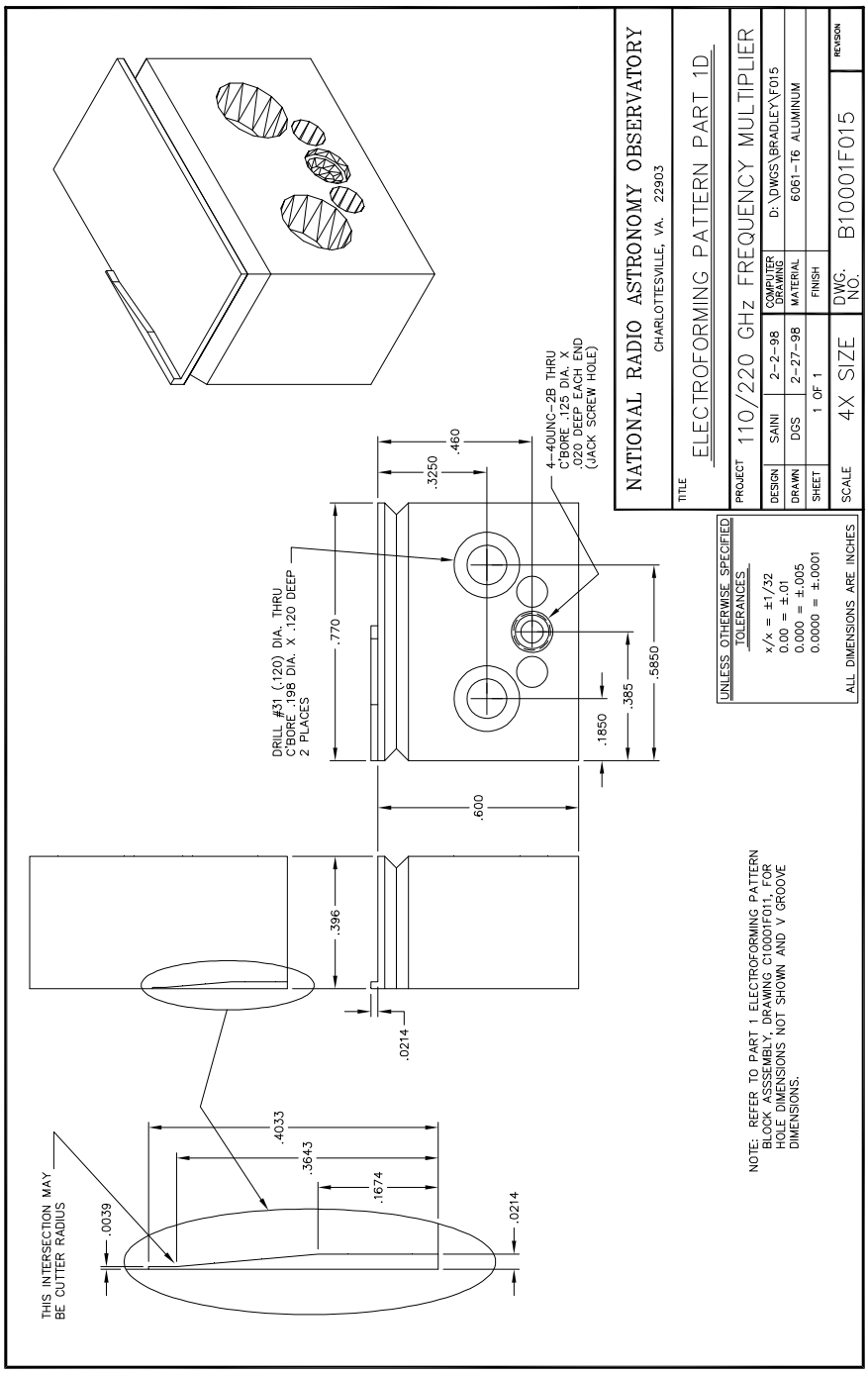


Figure D.24: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 1D.

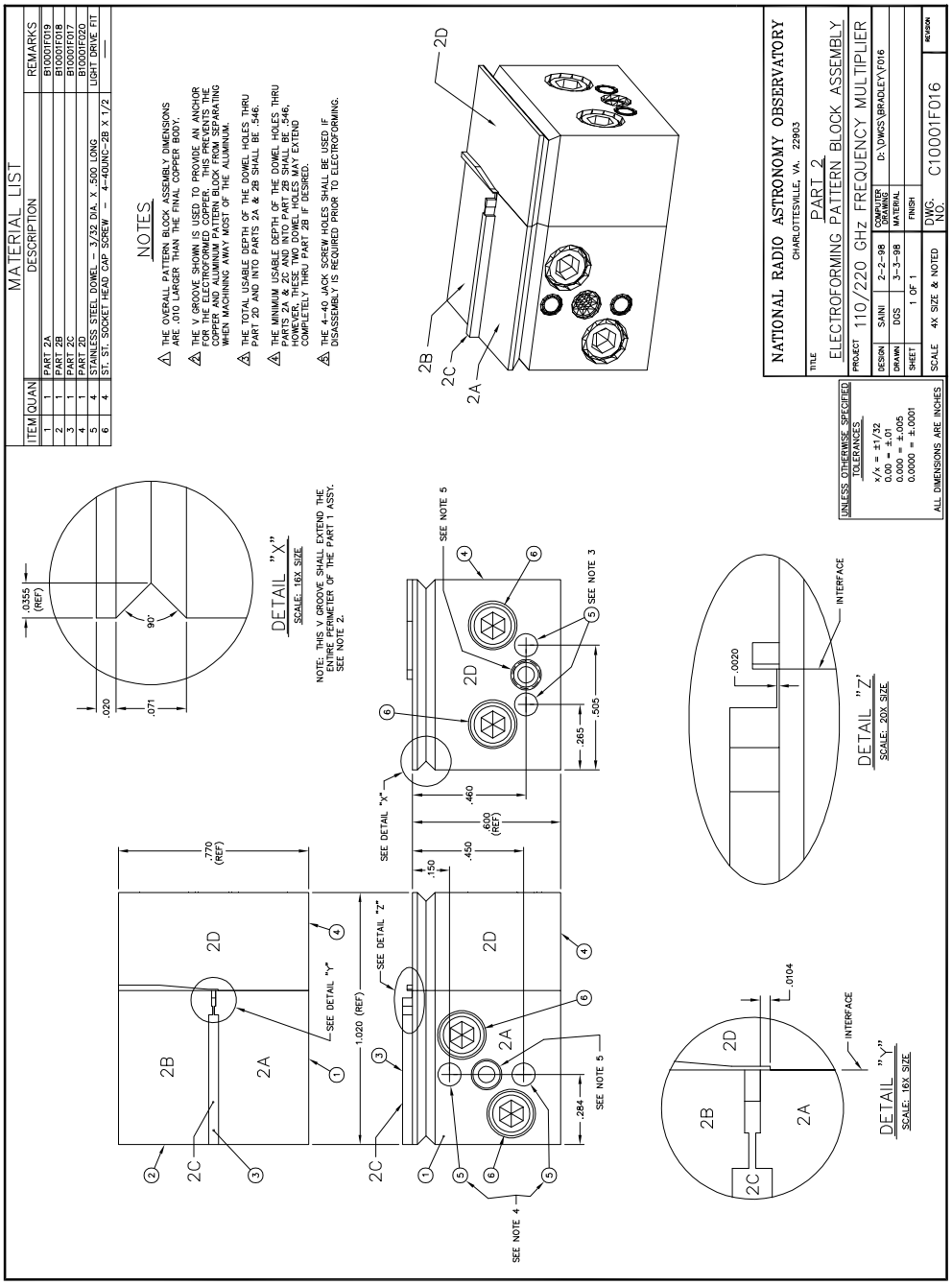


Figure D.25: 110/220 GHz frequency doubler: Assembly of the mandrel components 2A through 2D. This mandrel was used for electroforming part 2 of the split block.

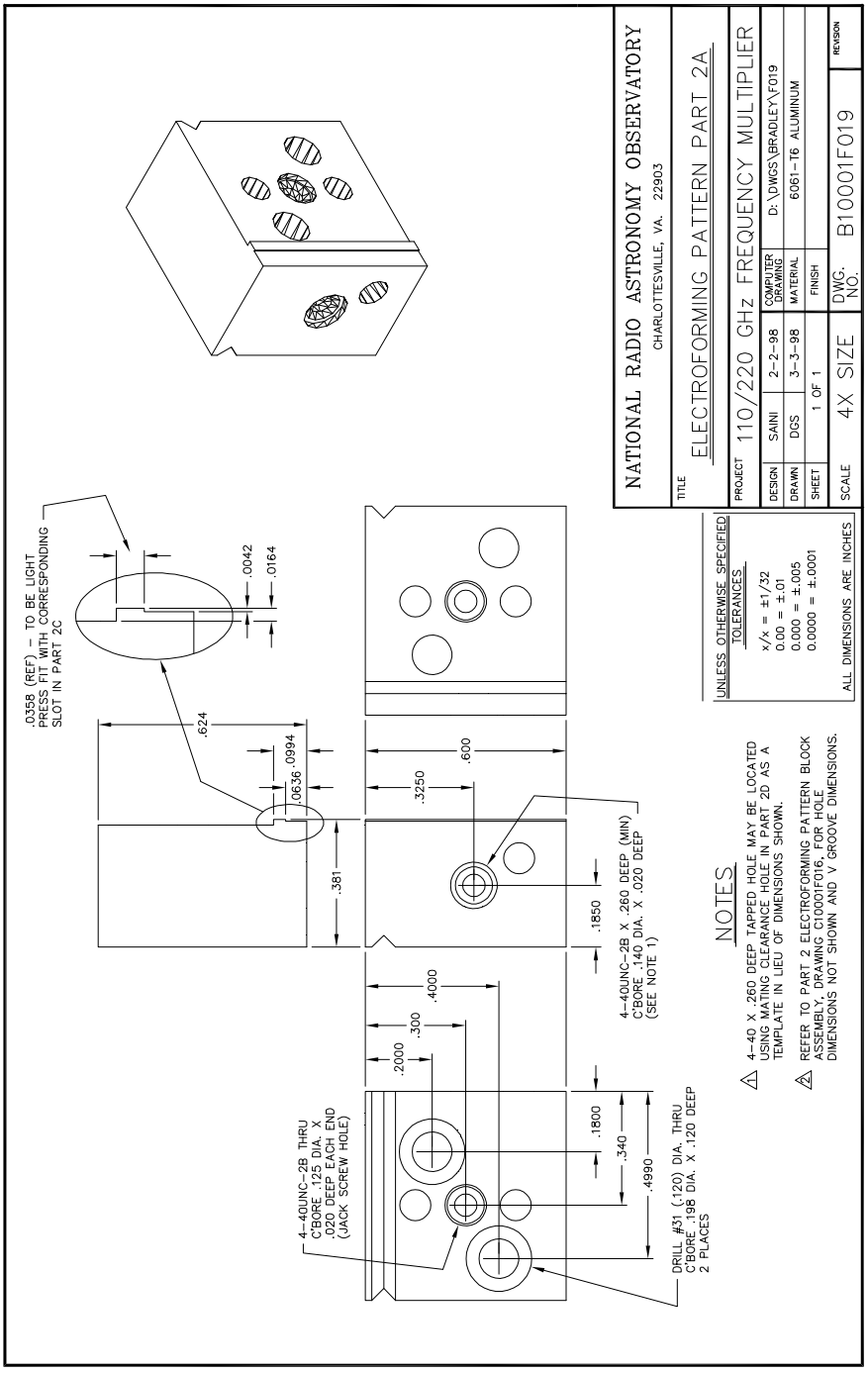


Figure D.26: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 2A.

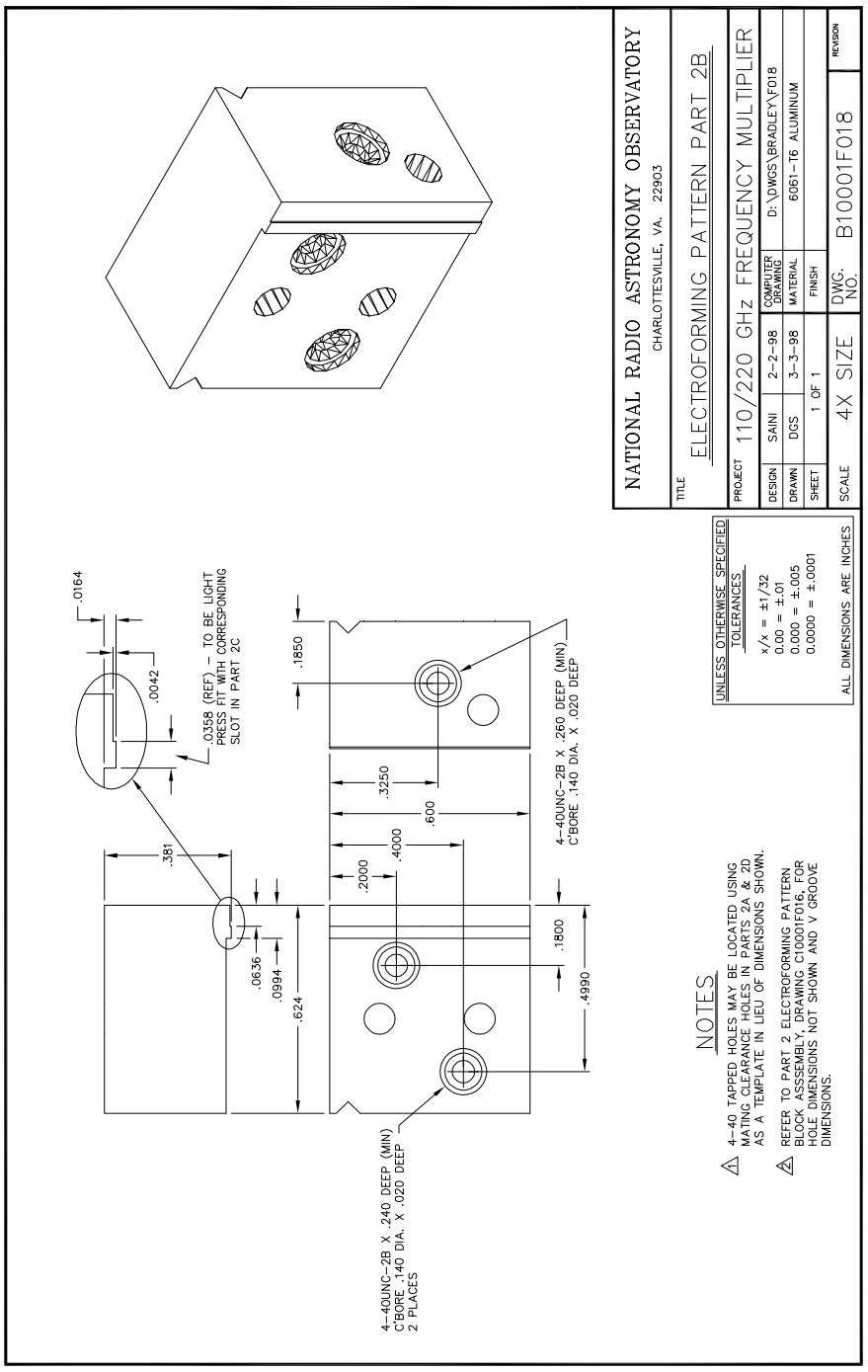


Figure D.27: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 2B.

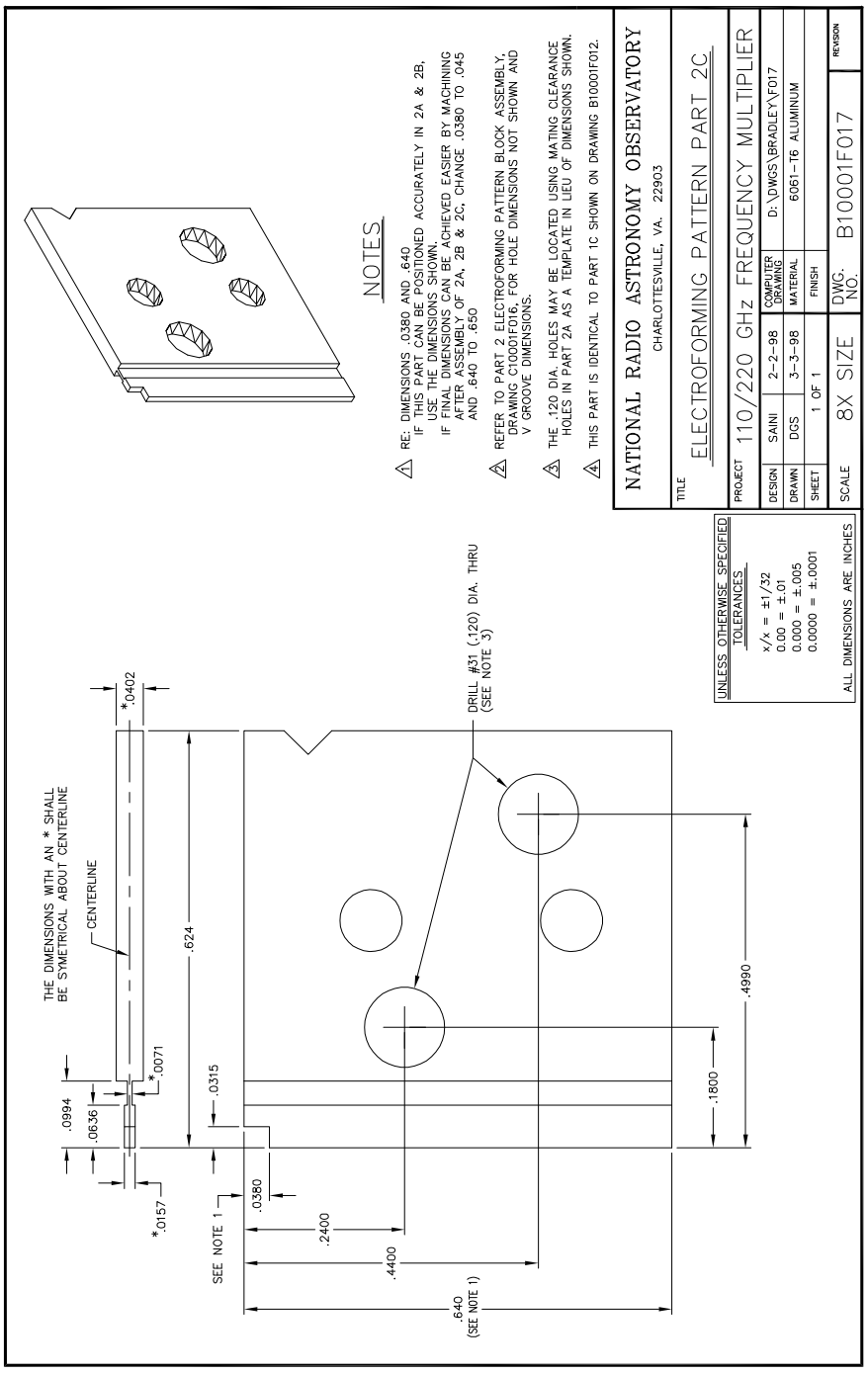


Figure D.28: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 2C.

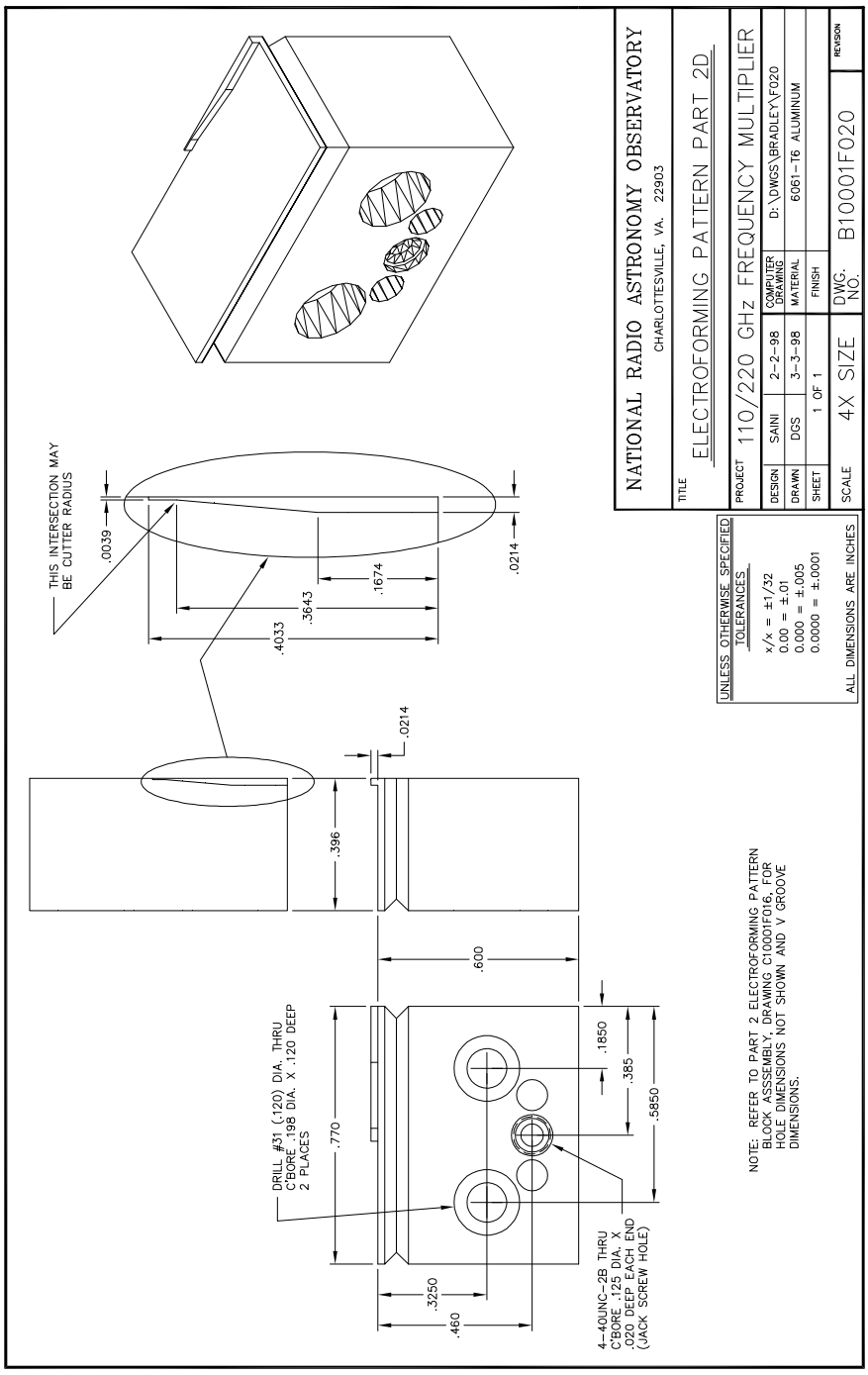


Figure D.29: 110/220 GHz frequency doubler: Mechanical details of the mandrel part 2D.

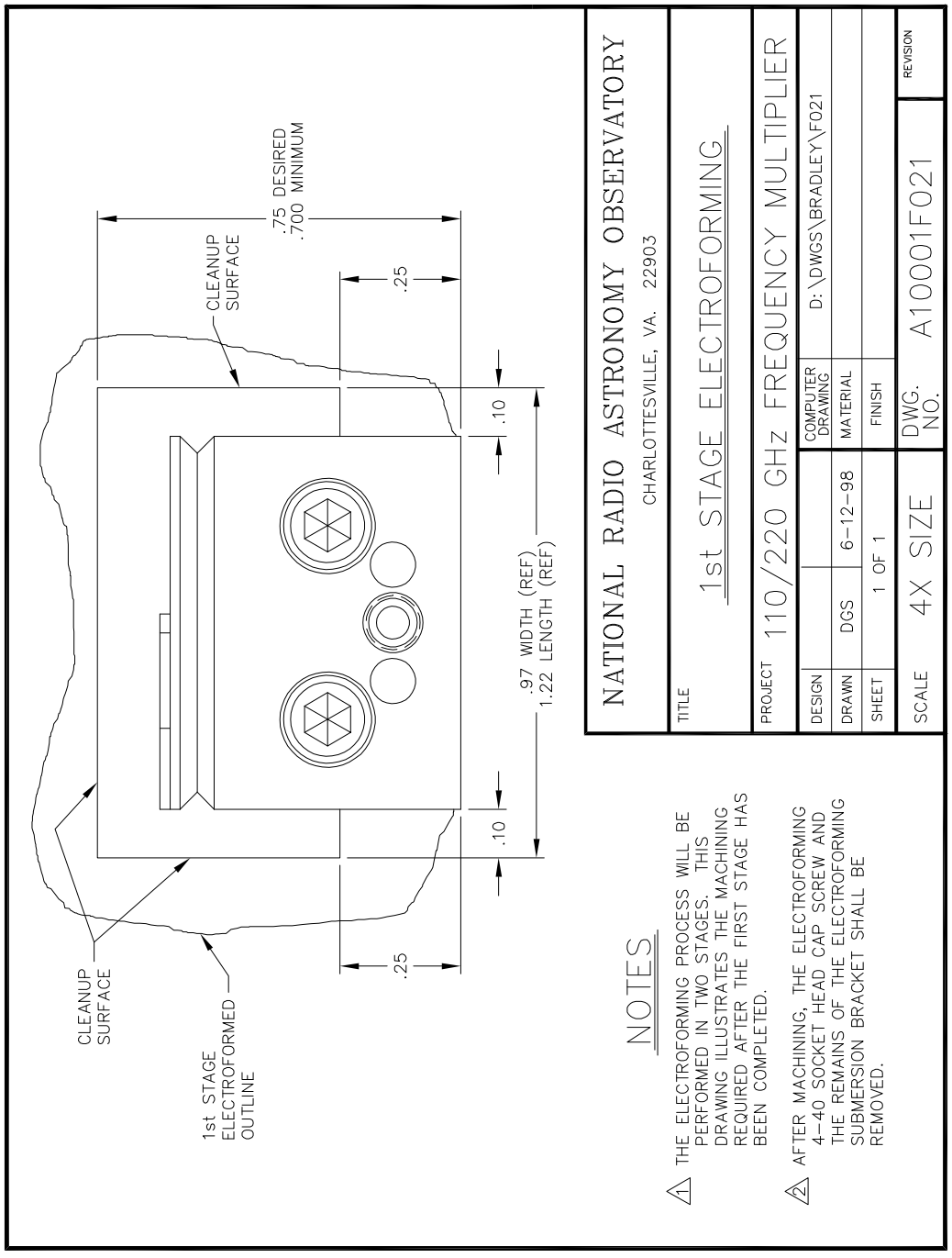


Figure D.30: 110/220 GHz frequency doubler: Details of the machining needed after completion of the first stage of electroforming.

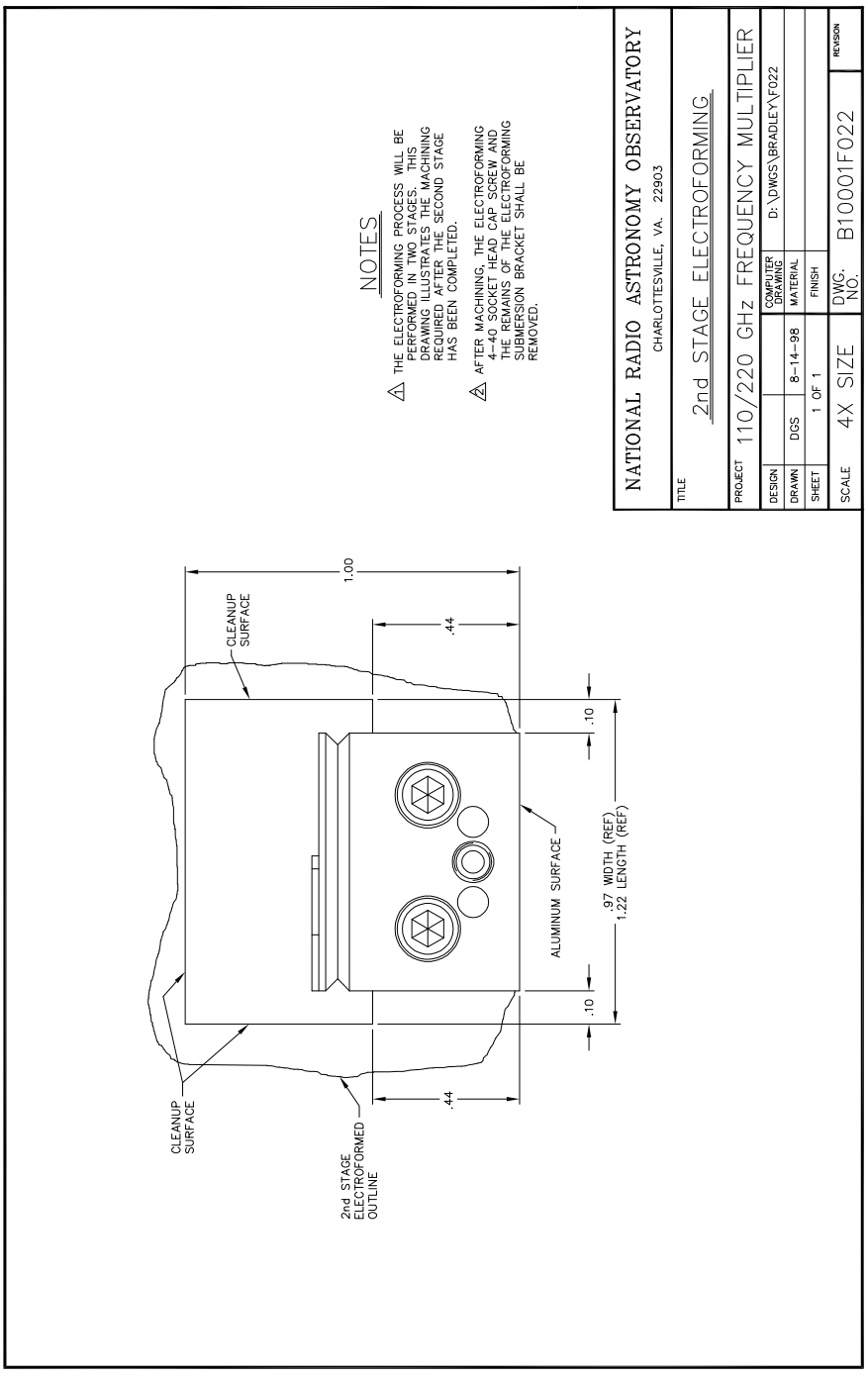


Figure D.31: 110/220 GHz frequency doubler: Details of the machining needed after completion of the second and final stage of electroforming.

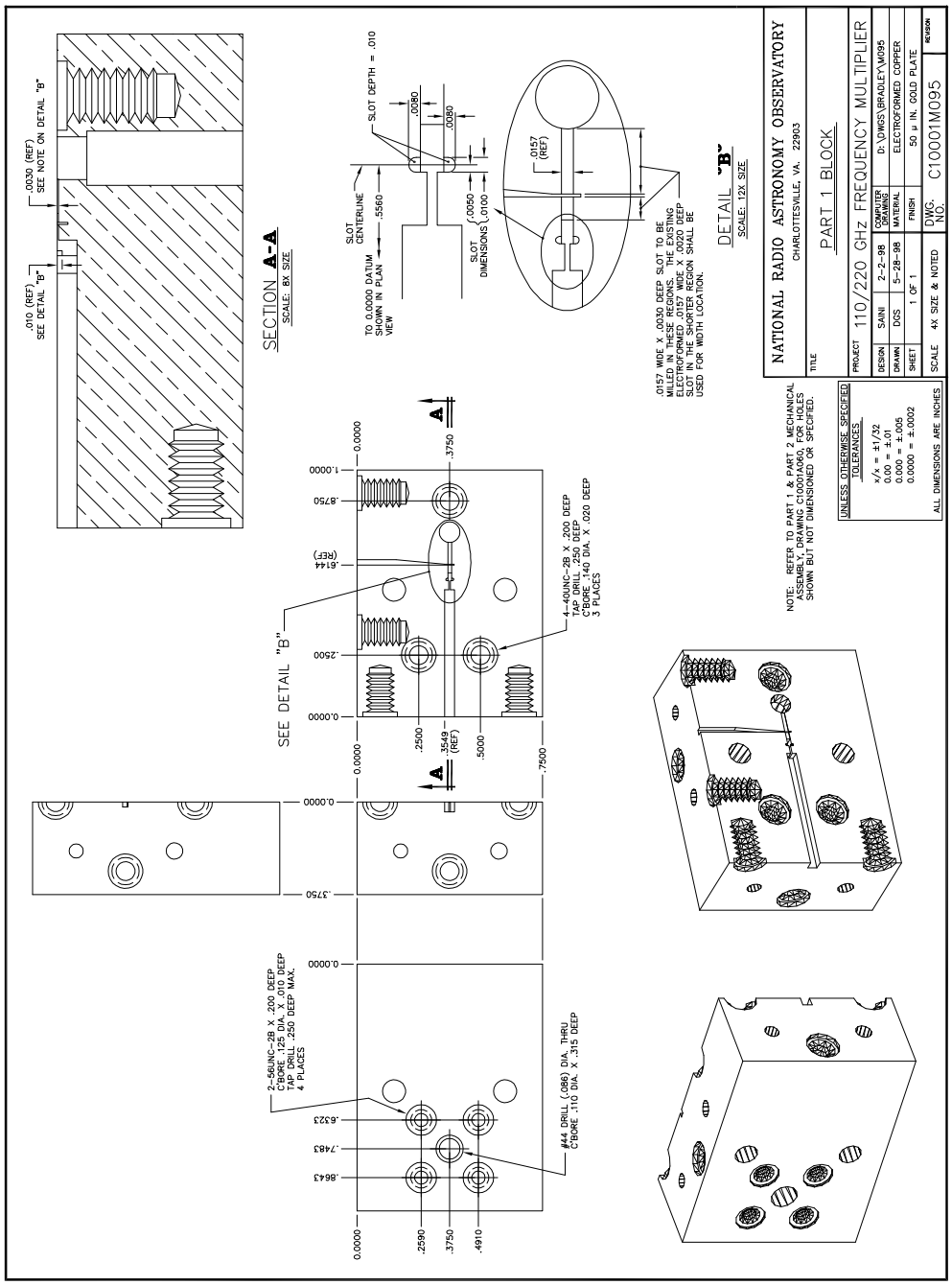


Figure D.32: 110/220 GHz frequency doubler: Mechanical details of part 1 of the two piece split block.

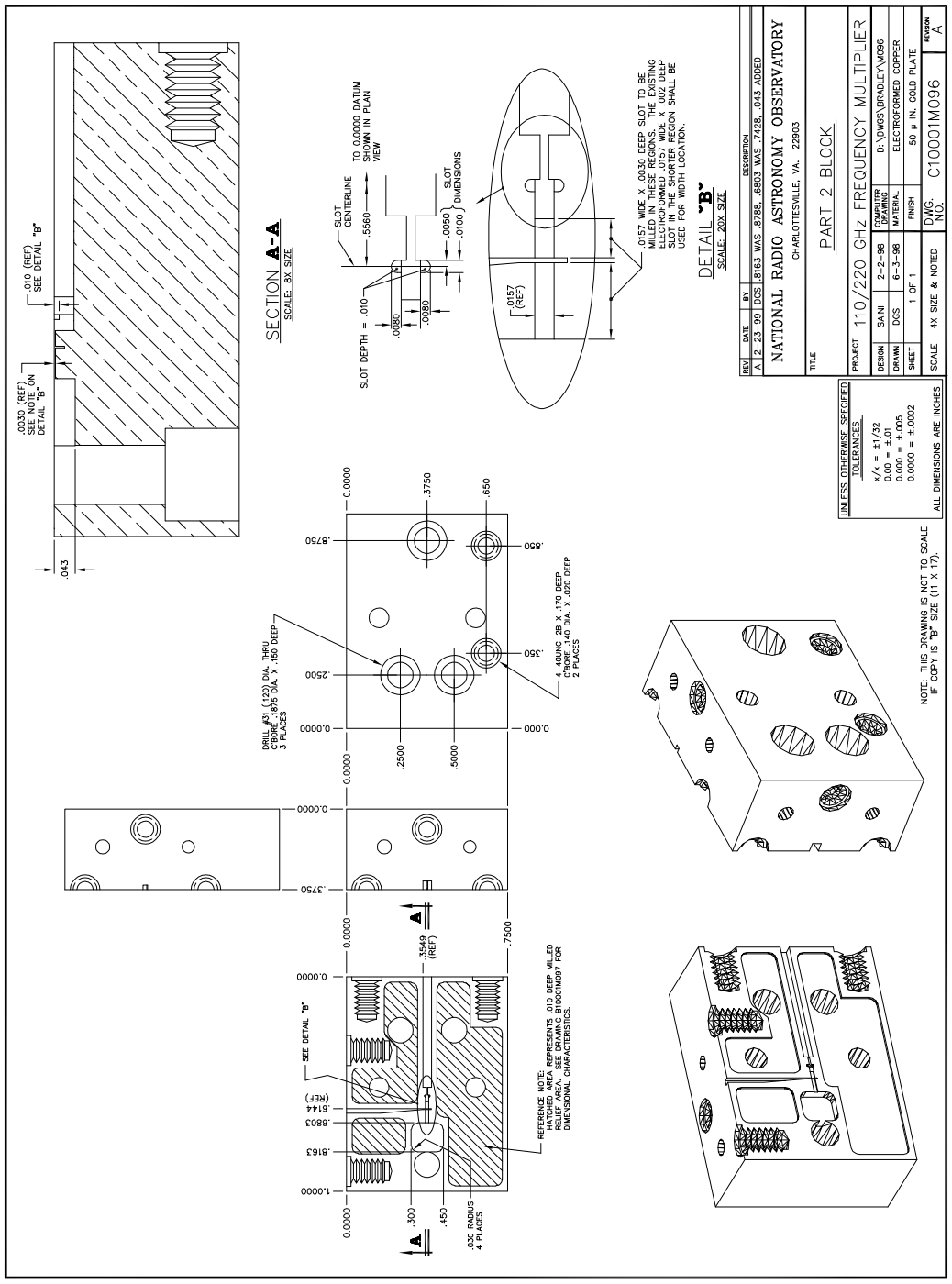


Figure D.33: 110/220 GHz frequency doubler: Mechanical details of part 2 of the two piece split block.

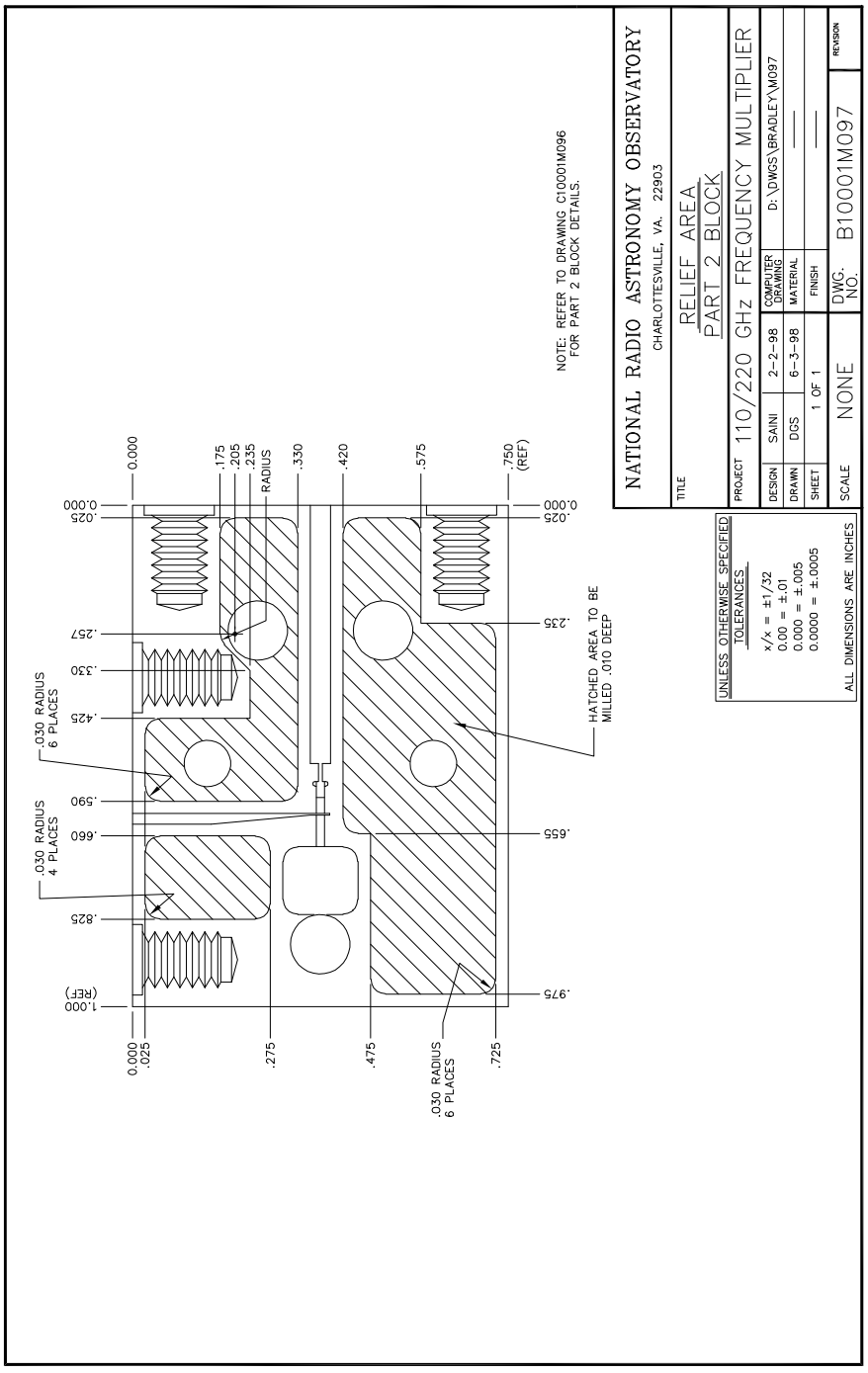


Figure D.34: 110/220 GHz frequency doubler: Location of the relief area in one of the halves (part 2) of the two piece split block.

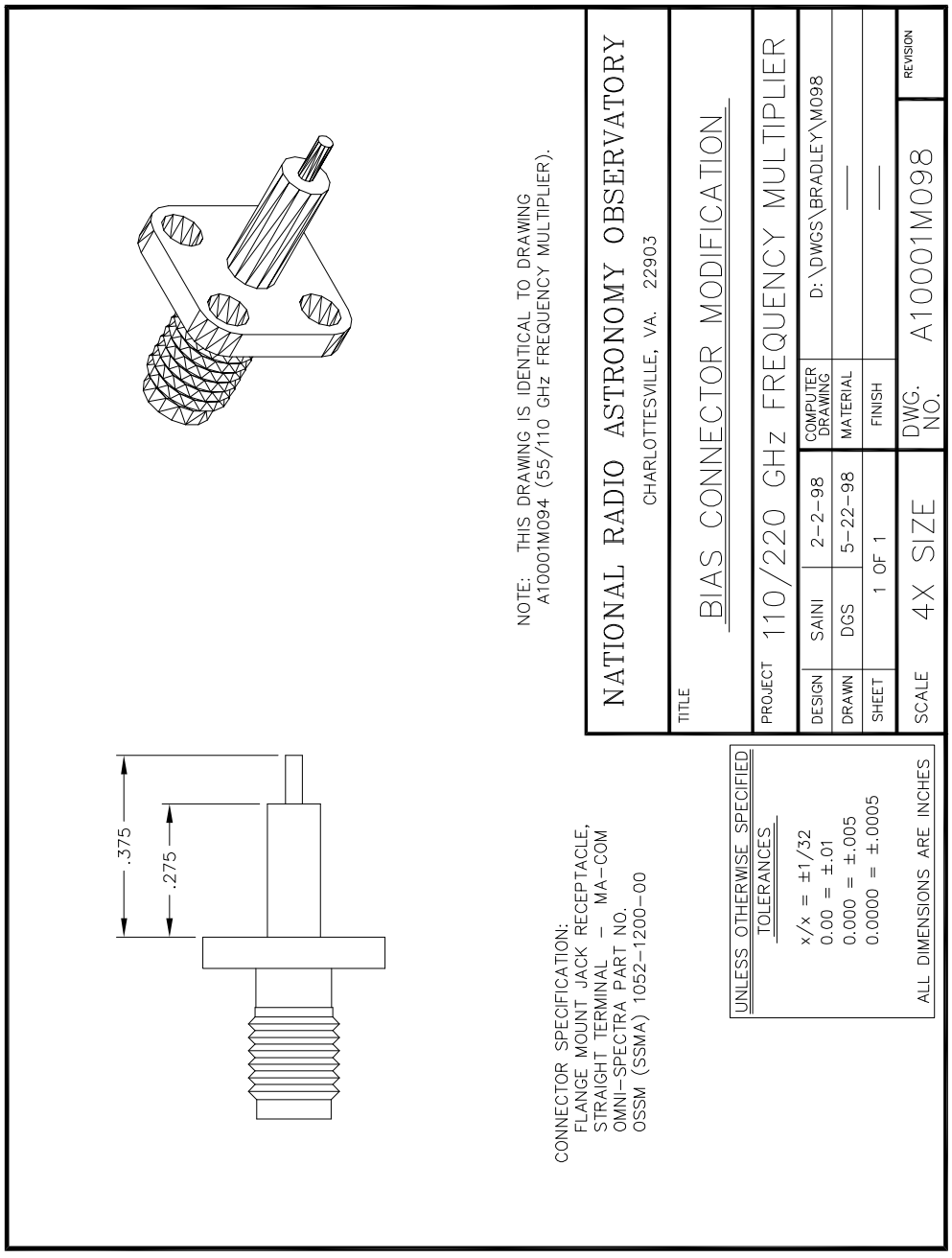


Figure D.35: 110/220 GHz frequency doubler: Details of the modified SSMA flange mount jack receptacle used as the DC bias connector.

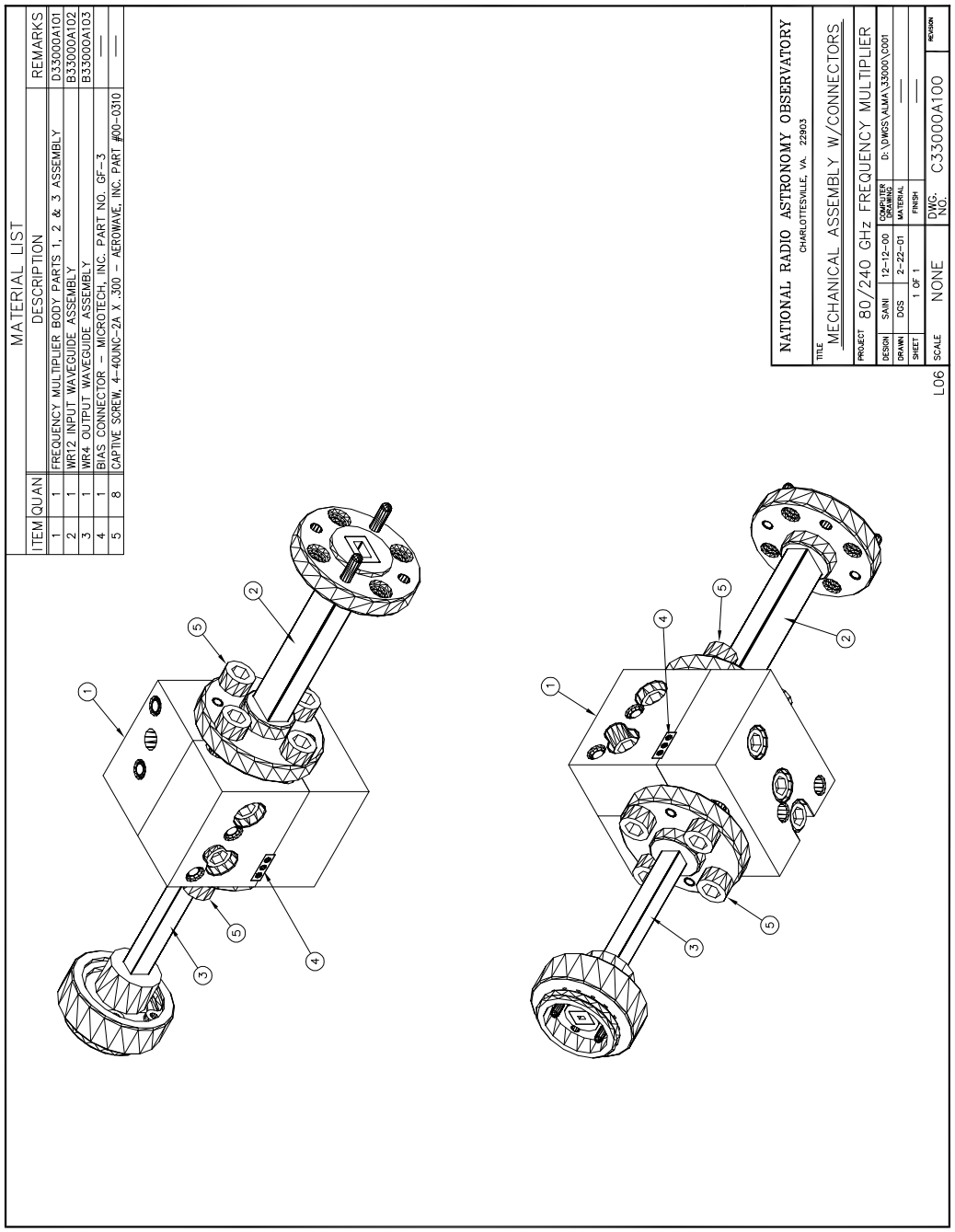


Figure D.36: 80/240 GHz frequency tripler, version 1: Mechanical assembly of the three piece block showing the DC bias connector and the waveguide flange adapters.

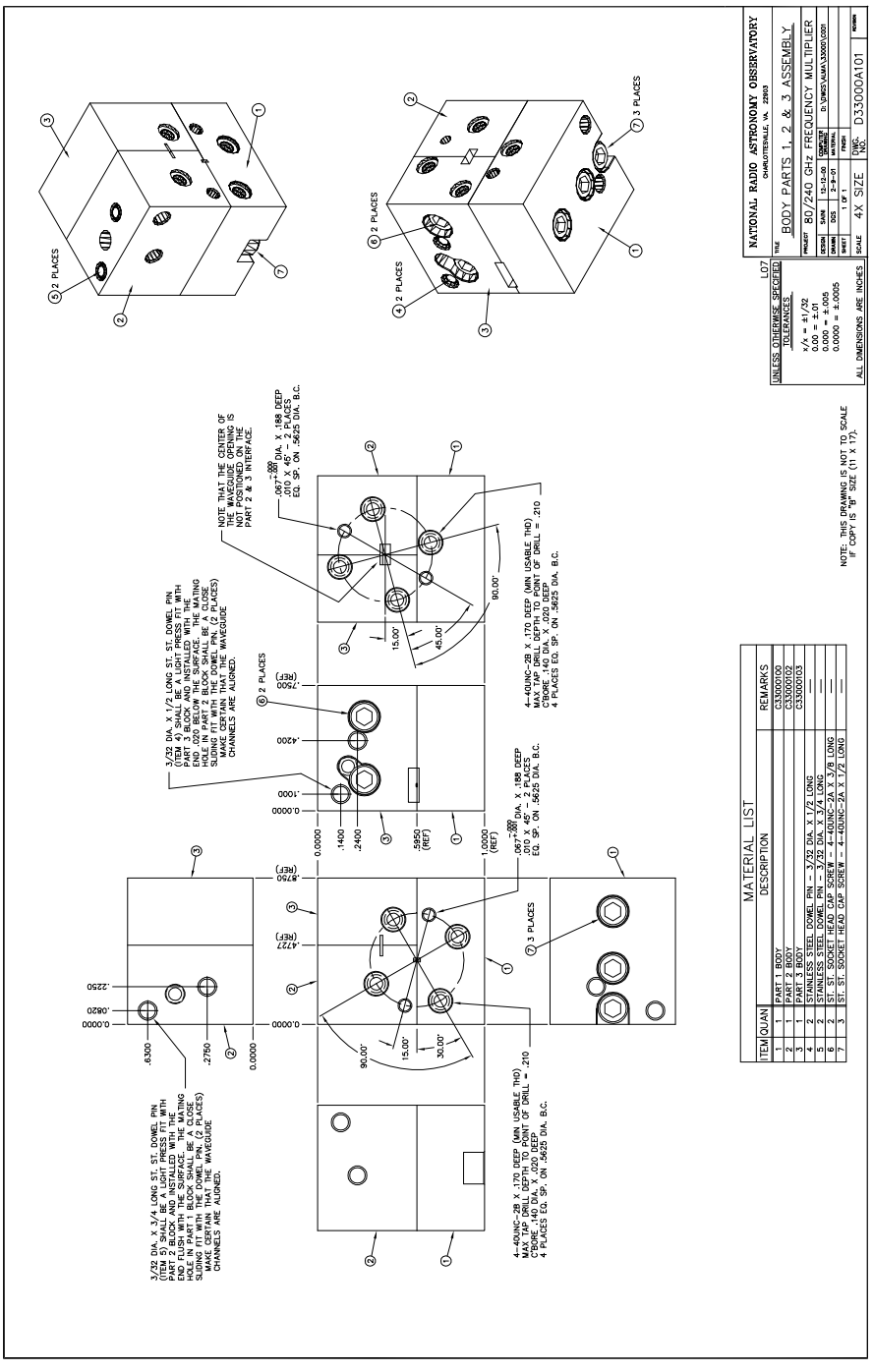


Figure D.37: 80/240 GHz frequency tripler, version 1: External mechanical assembly of parts 1, 2 and 3 comprising the metal block.

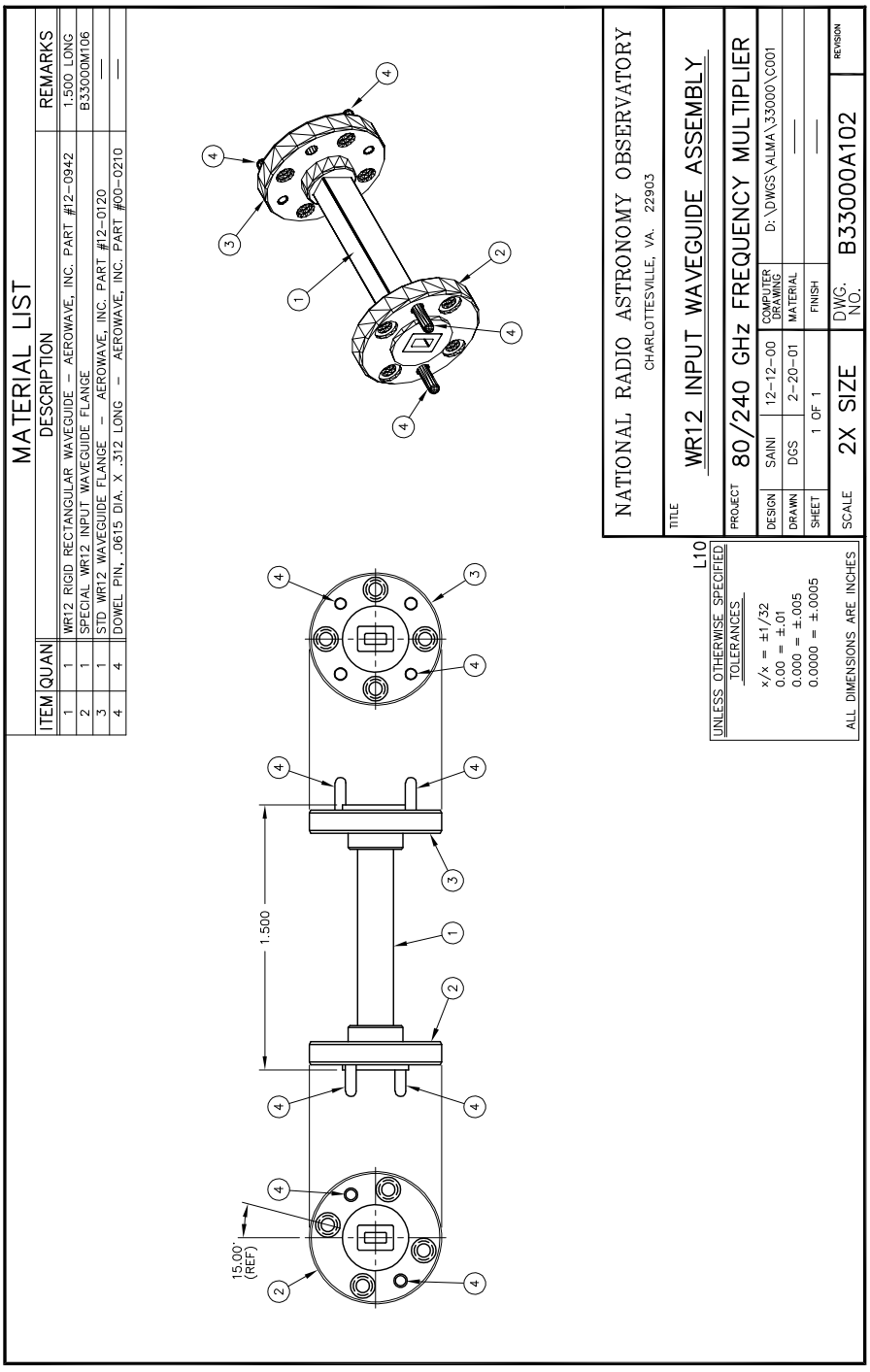


Figure D.38: 80/240 GHz frequency tripler, version 1 and 2: WR-12 input waveguide flange adapter assembly.

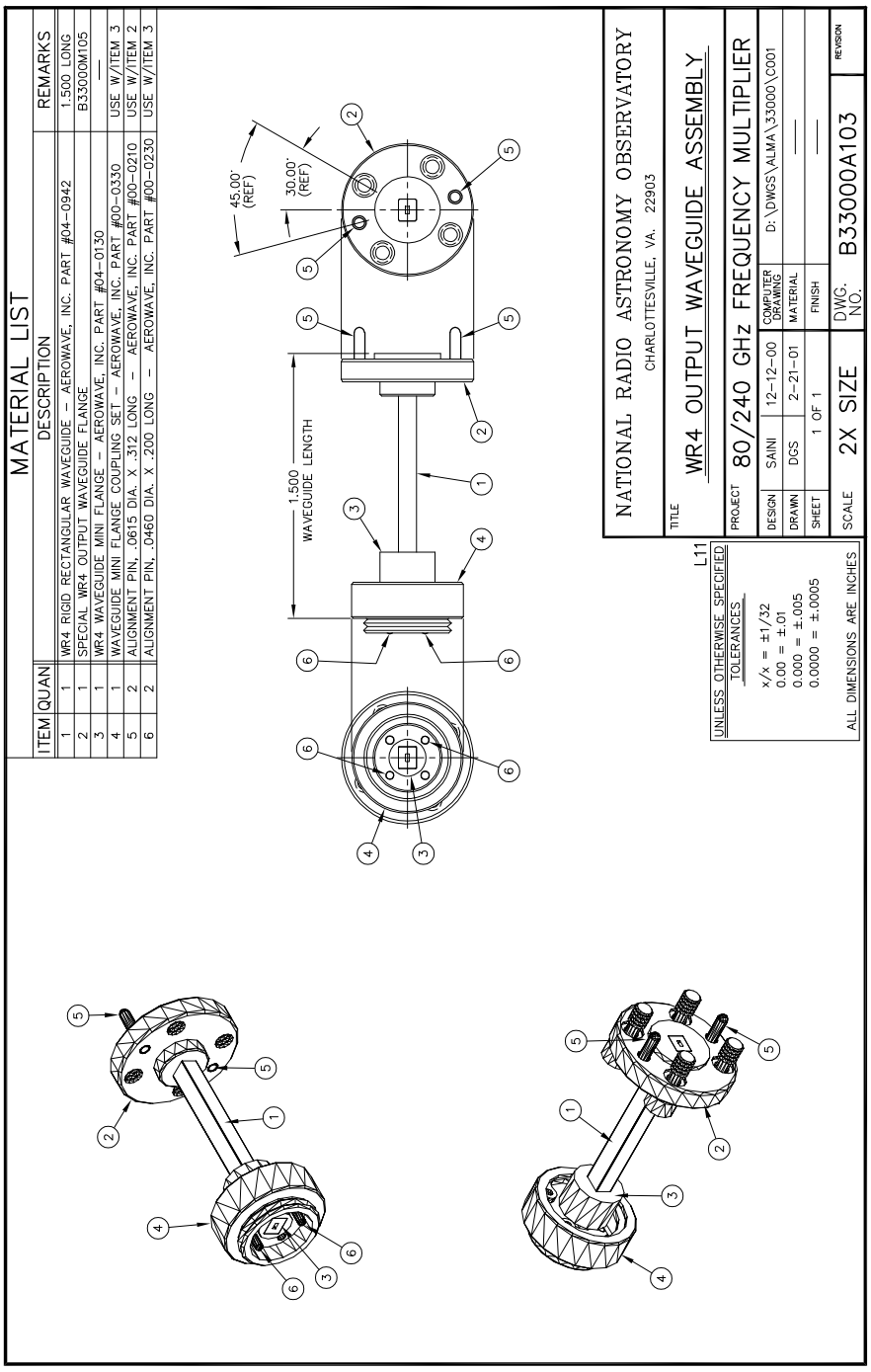


Figure D.39: 80/240 GHz frequency tripler, version 1 and 2: WR-4 output waveguide flange adapter assembly.

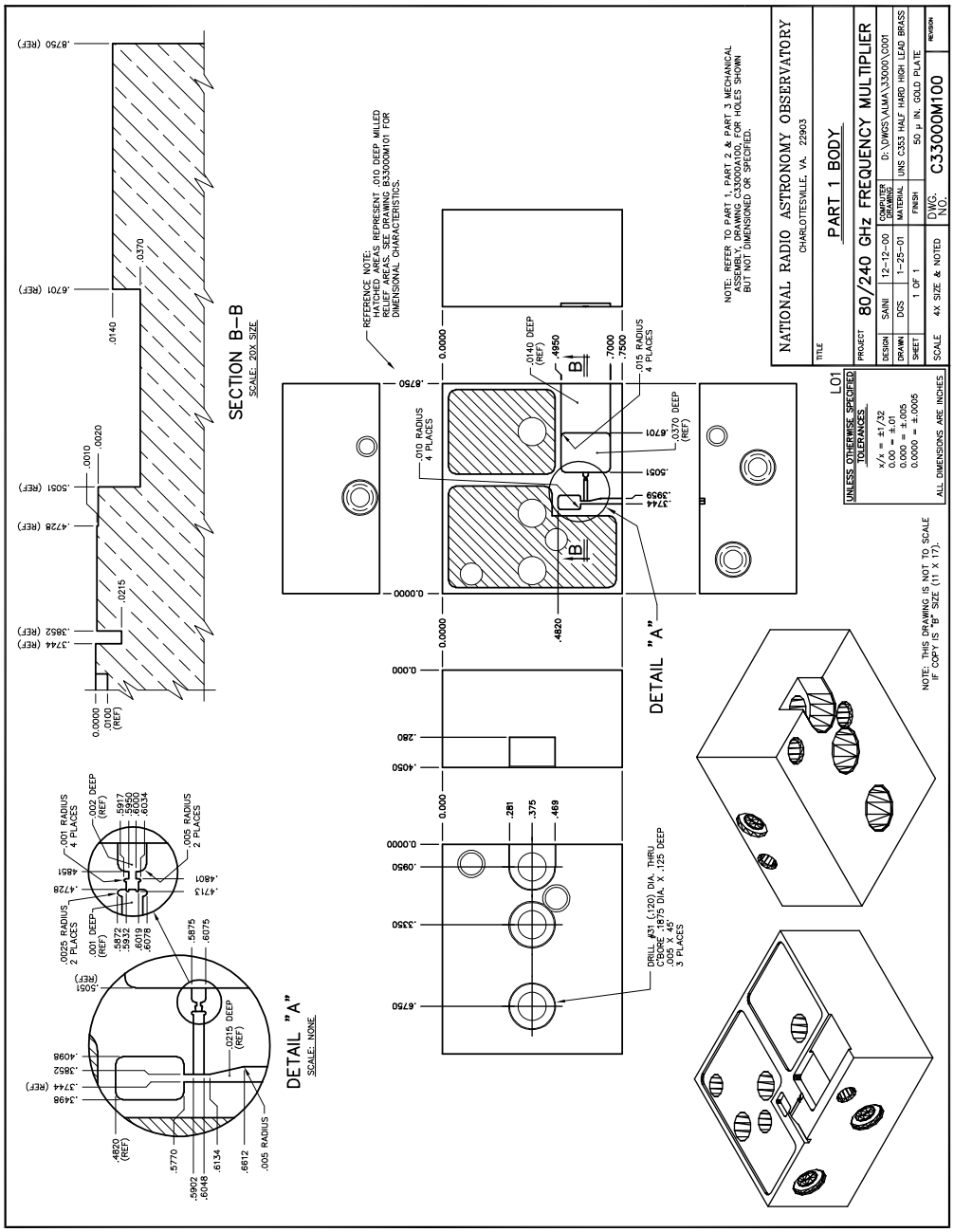


Figure D.40: 80/240 GHz frequency tripler, version 1: Mechanical details of part 1 of the three piece metal block.

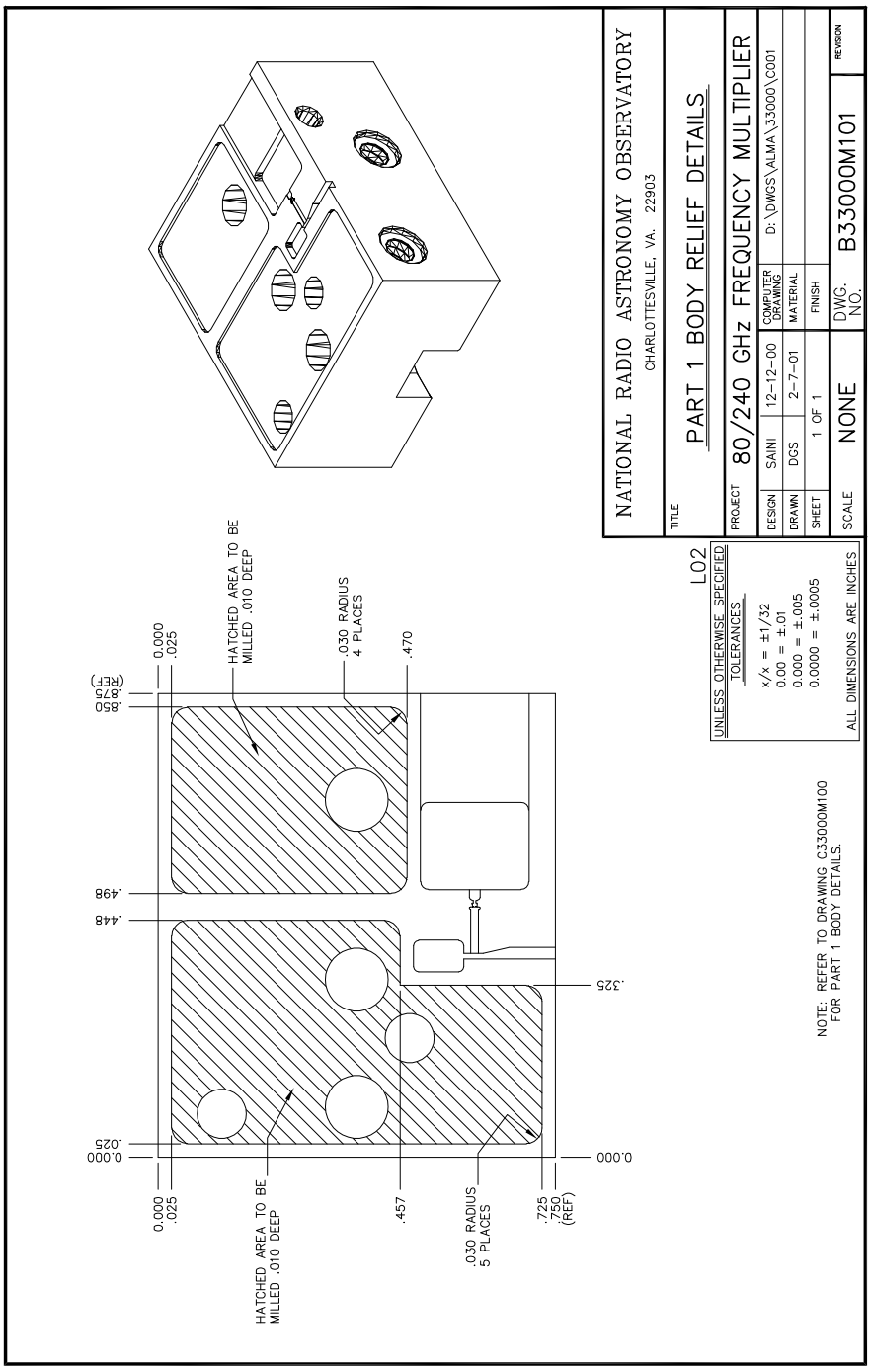


Figure D.41: 80/240 GHz frequency tripler, version 1: Location of the relief area in part 1 of the three piece metal block.

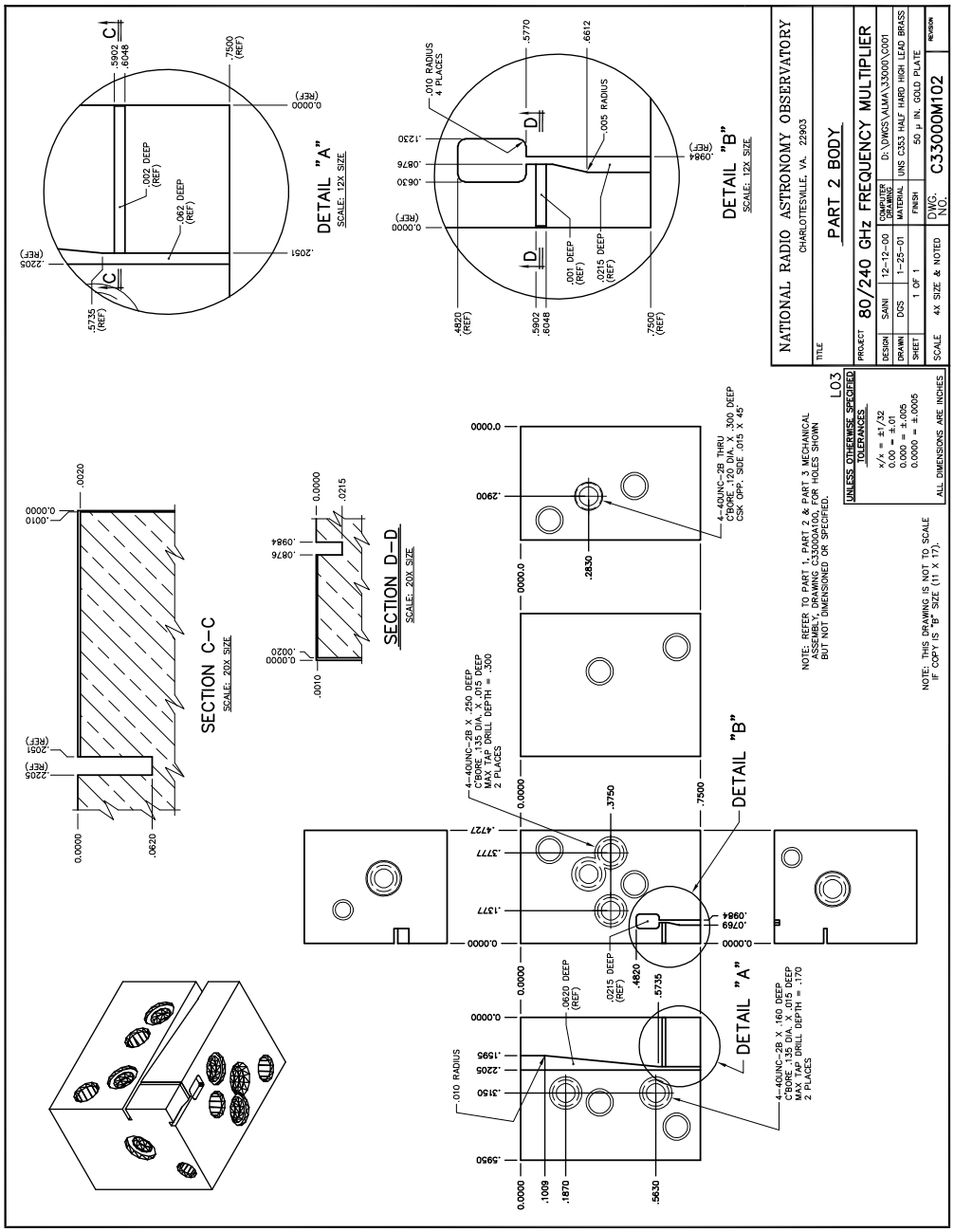


Figure D.42: 80/240 GHz frequency tripler, version 1: Mechanical details of part 2 of the three piece metal block.

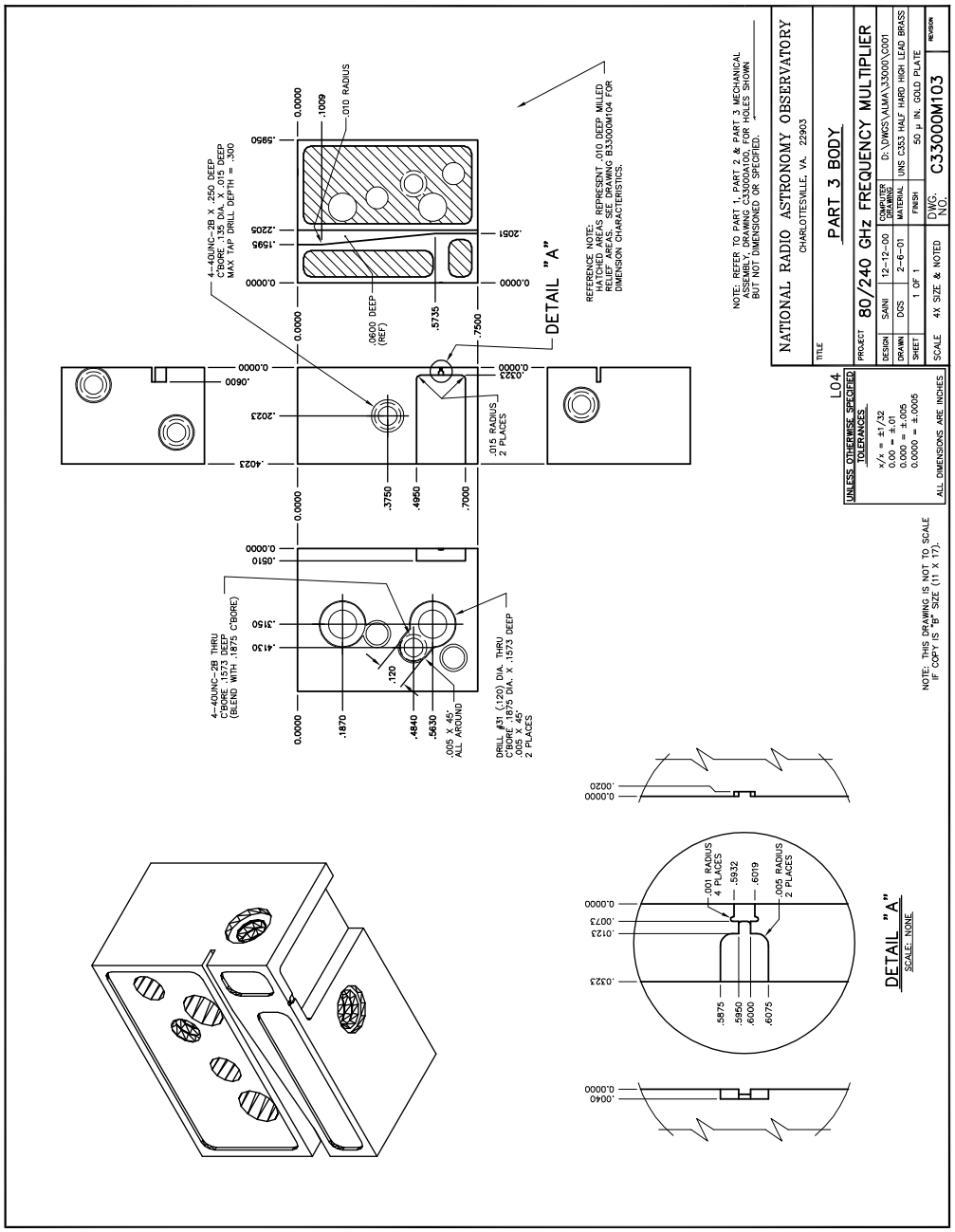


Figure D.43: 80/240 GHz frequency tripler, version 1: Mechanical details of part 3 of the three piece metal block.

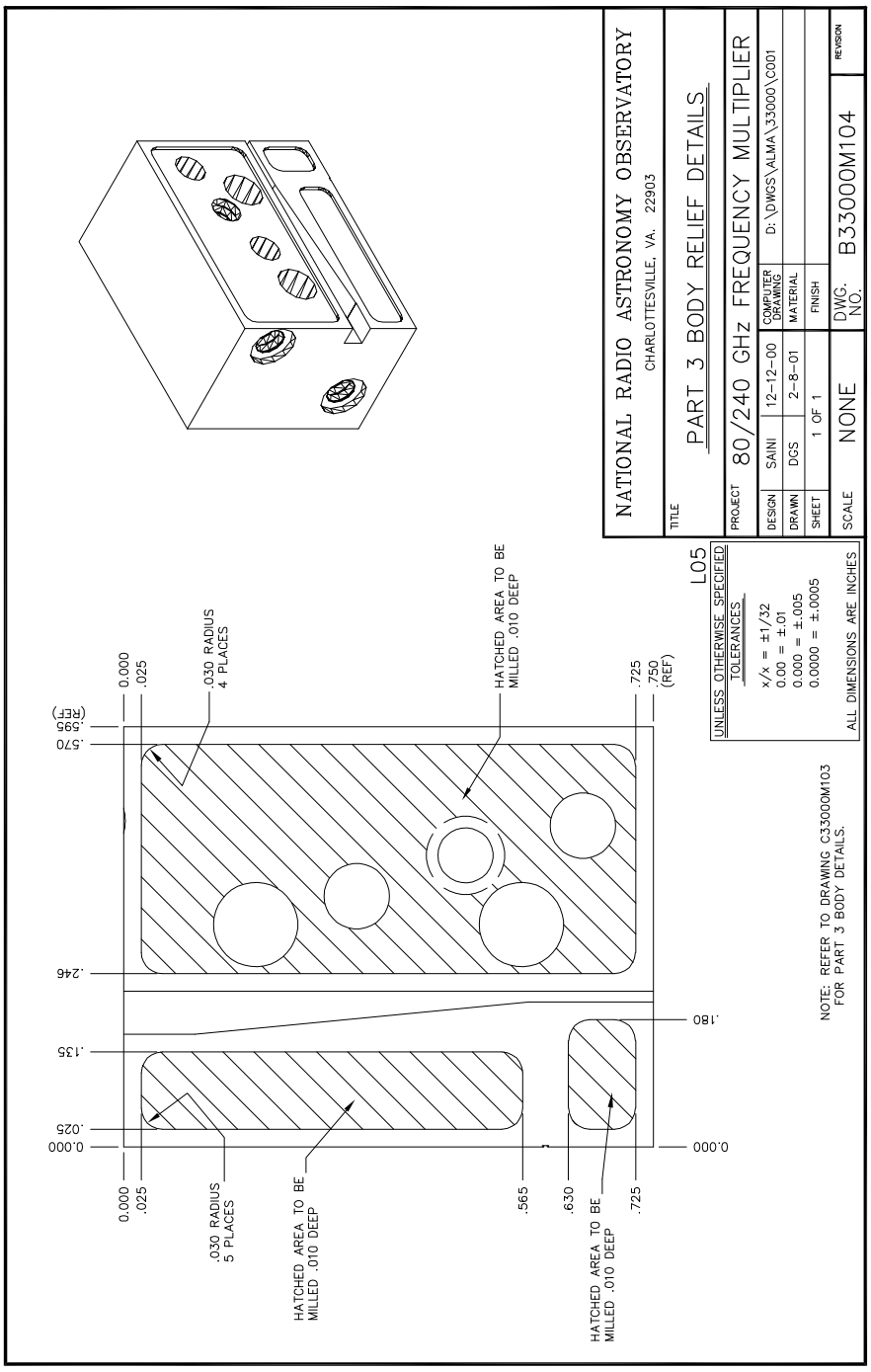


Figure D.44: 80/240 GHz frequency tripler, version 1: Location of the relief area in part 3 of the three piece metal block.

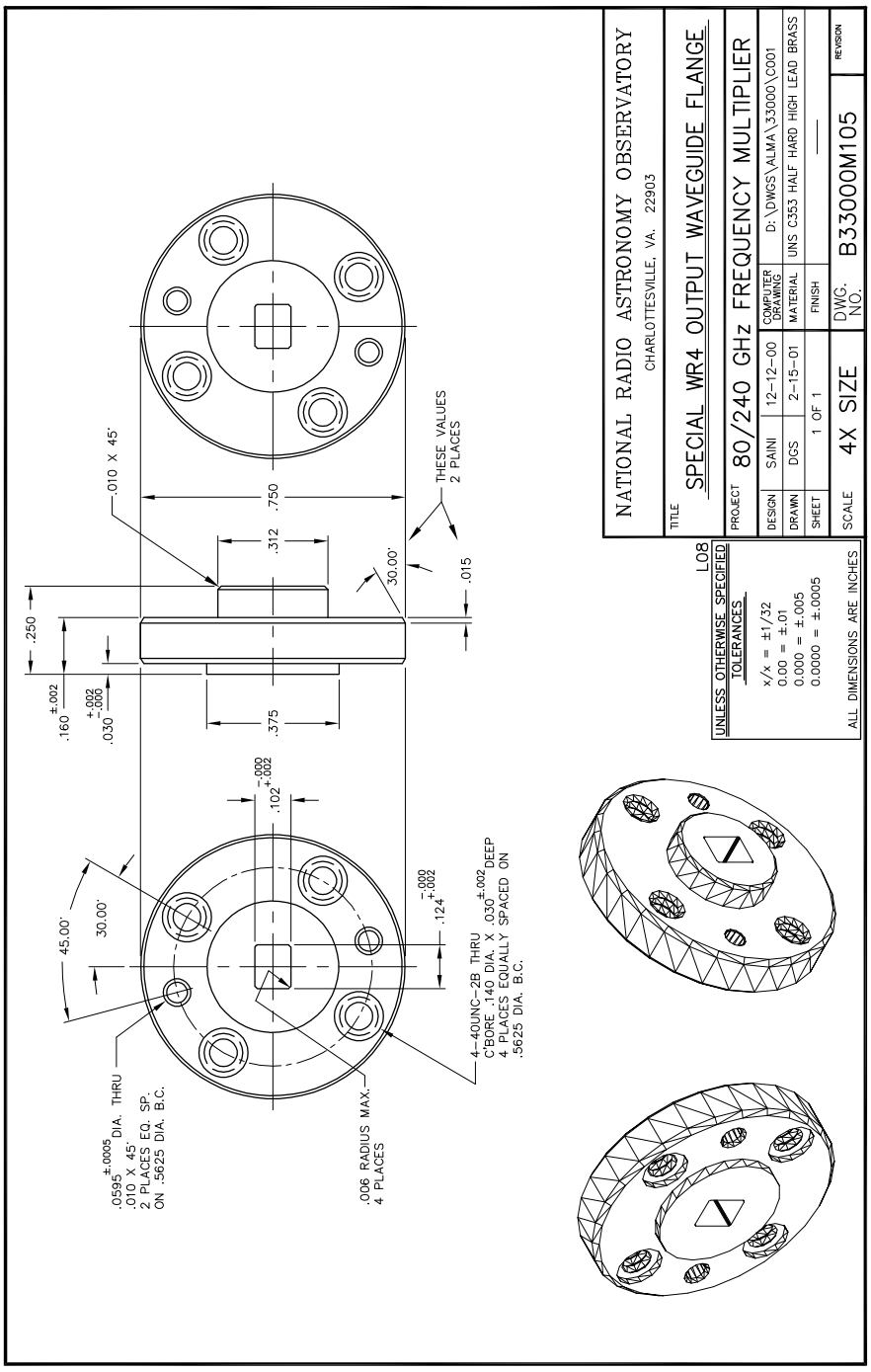


Figure D.45: 80/240 GHz frequency tripler, version 1 and 2: Mechanical details of the special WR-4 output waveguide flange.

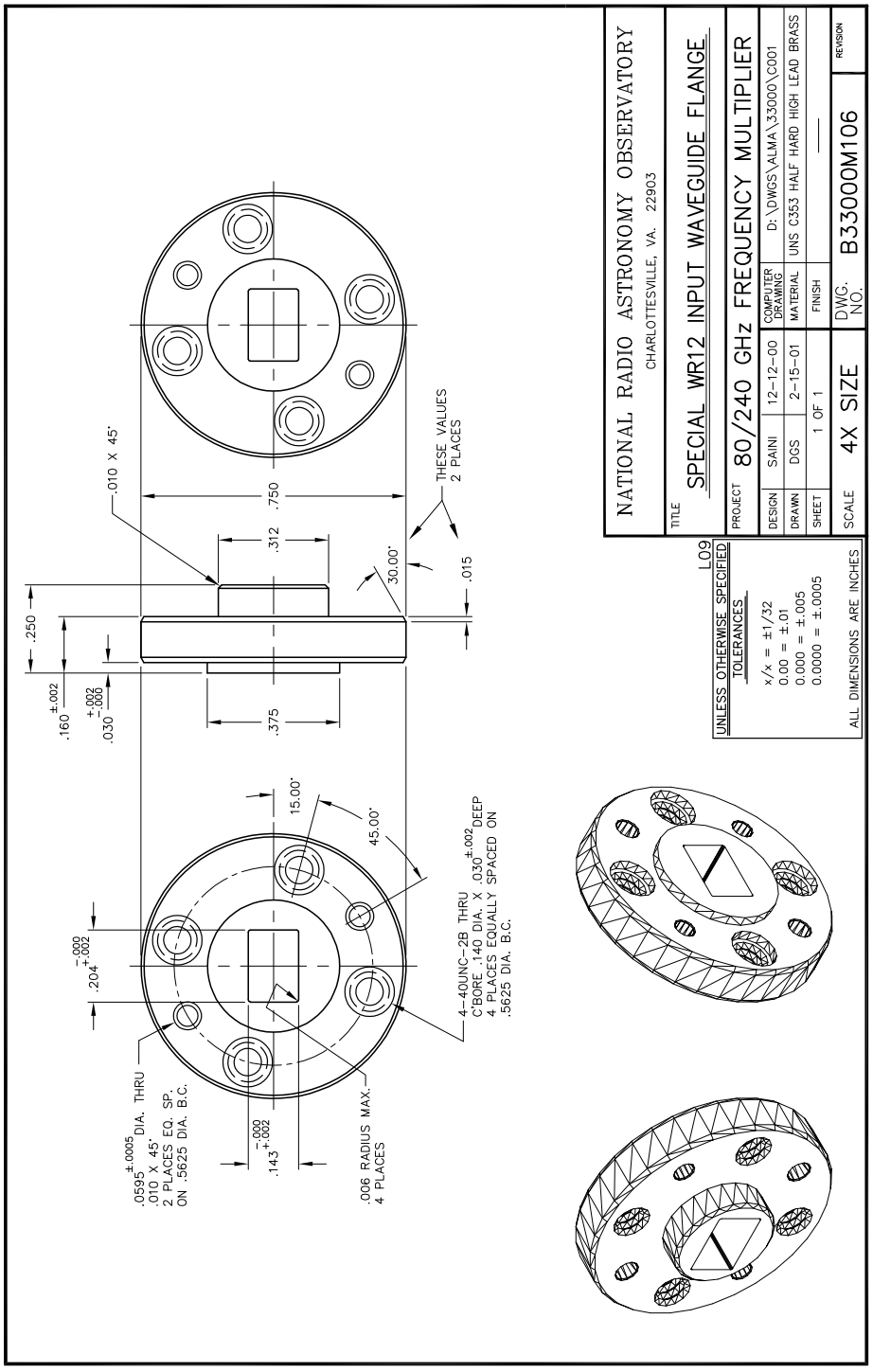


Figure D.46: 80/240 GHz frequency tripler, version 1 and 2: Mechanical details of the special WR-12 input waveguide flange.

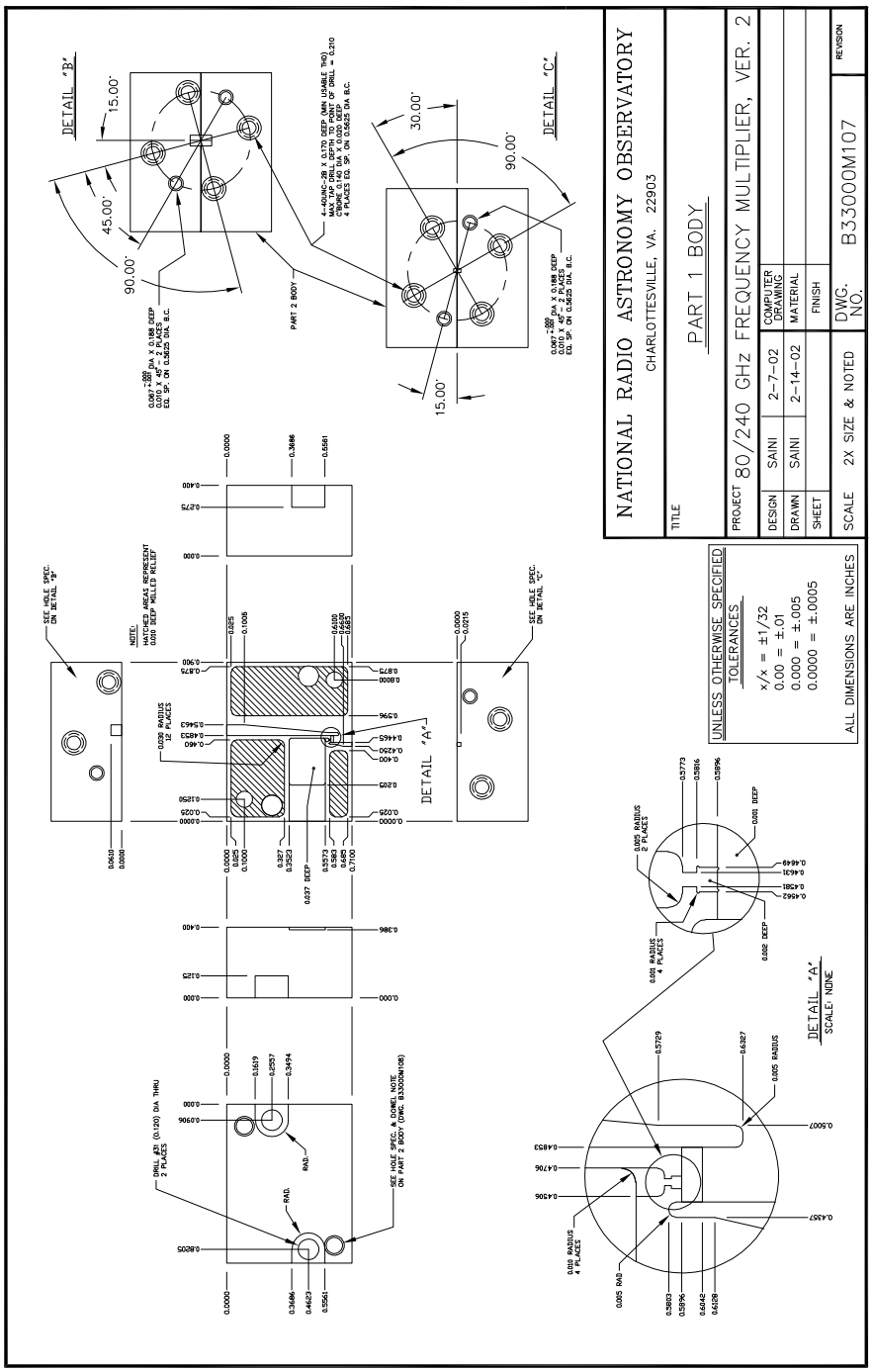


Figure D.47: 80/240 GHz frequency tripler, version 2: Mechanical details of part 1 of the two piece split block.

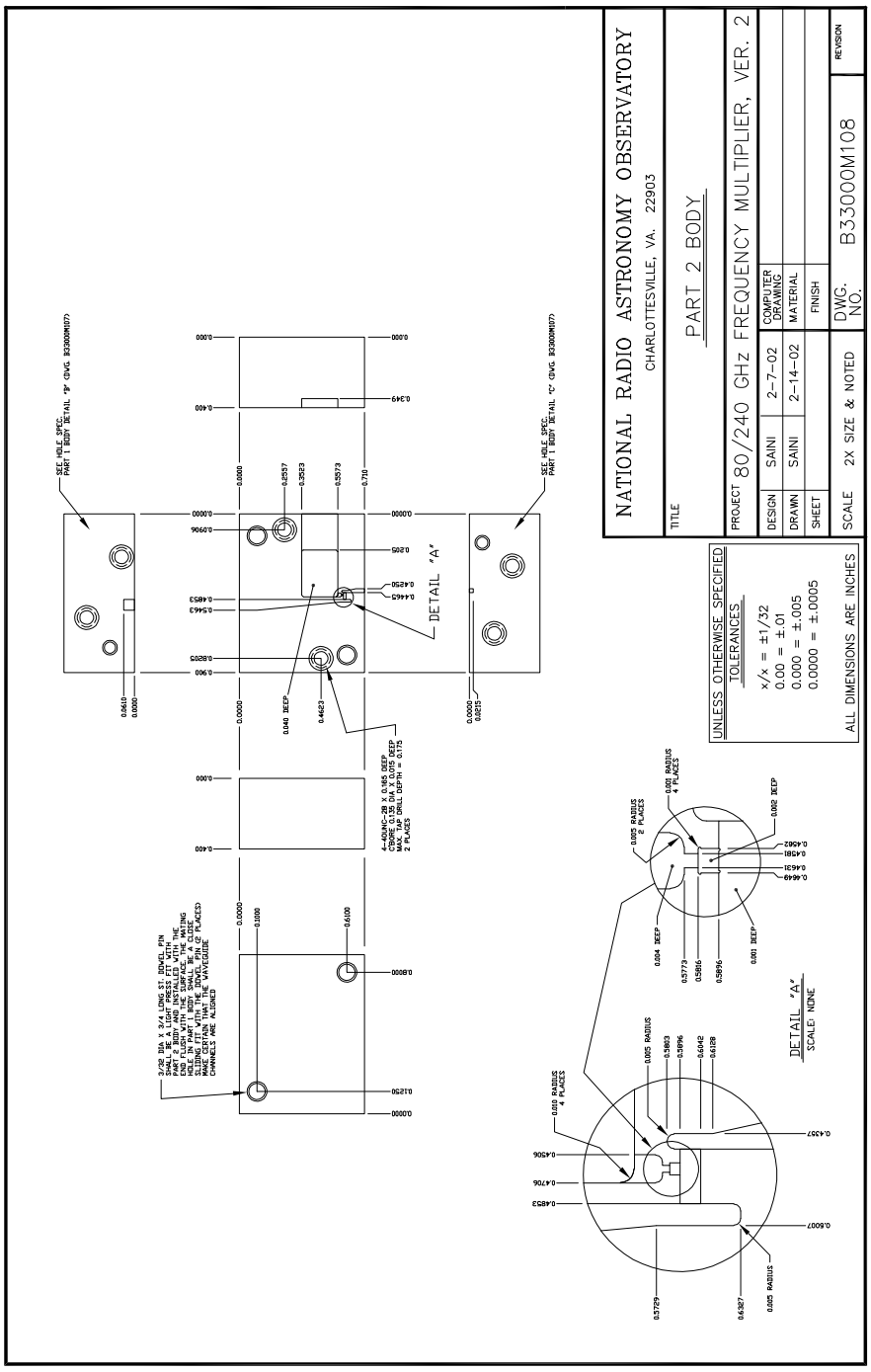


Figure D.48: 80/240 GHz frequency tripler, version 2: Mechanical details of part 2 of the two piece split block.

Appendix E

Assembly Procedures

The assembly procedures for the various frequency multiplier blocks are described in this appendix.

E.1 Assembly of the 55/110 GHz Frequency Doubler

The technique of attaching the diode array to the planar quartz circuit and their subsequent integration into the metal housing is described.

The first step in assembling the 55/110 GHz frequency doubler was to attach three bond wires to the quartz circuit as shown in Figure-E.1. The

quartz circuit had to be mounted on top of a small metal piece using G-wax for this purpose. The metal piece was then mounted on the wire-bonder stage and 0.7 mil diameter bond wires attached at appropriate locations. The free hanging ends of two of the three the bond wires (located to the right in Figure-E.1) would be eventually attached to appropriate spots on the metal housing to provide RF and DC ground for the diode array. These two bond wires were made to extend out about 10 mils from the quartz circuit. The third bond wire, meant to be connected to the DC bias connector, was made to be substantially longer (about 10 mm).

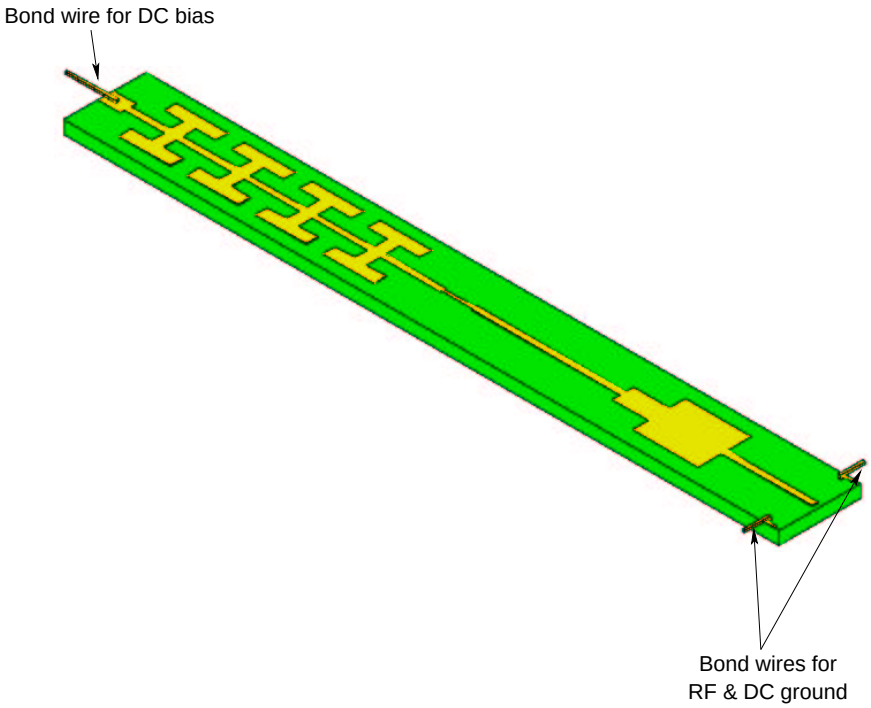


Figure E.1: Bond wire locations on the 55/110 GHz frequency doubler quartz circuit.

The metal piece with the quartz circuit was subsequently mounted on top of a miniature hot plate and a small amount of a high temperature solder

(Indalloy #2, melting point $149^oC - 155^oC$, from Indium Corporation of America [148]) was applied at of each of the three wire bond locations. This served to mechanically reinforce the wire bonds. Solder flux (Supersafe No. 30, from Superior Flux and Mfg. Co. [149]) was used to promote solder flow.

The quartz circuit was then removed from the metal piece by dissolving the G-wax in Acetone and then re-mounted on a glass slide, again using G-wax. Small amounts of a low temperature solder (Indalloy #1, melting point $118^oC - 125^oC$, from Indium Corporation of America) was applied to the three points on the circuit metalization where the three pads of the varactor chip were to be attached, as shown in Figure-E.2. Solder flux, used to promote solder flow, was rinsed away by dipping the glass slide with the quartz circuit in warm DI-water. After blow drying the quartz circuit with compressed nitrogen, solder flux was re-applied to the now rounded solder "bumps". A UVA SB13T1 varactor chip was then flipped (metalized side facing down) and placed with its pads aligned with the location of the solder "bumps" as shown in Figure-E.3 and a micro-slide was placed on top to apply a downward pressure on the diode array and hold it in place. The glass slide was re-heated to melt the low temperature solder, but not affect the high temperature solder used to reinforce the wire bonds. Heating was discontinued when the solder began to re-flow and the circuit was cooled to prevent any thermal damage to the semiconductor and the Schottky junctions. The excess flux was subsequently rinsed away by dipping the glass slide in warm DI-water. The circuit with the attached diode array was then dislodged from the glass slide by dipping it in Acetone and was ready to be mounted into the metal housing.

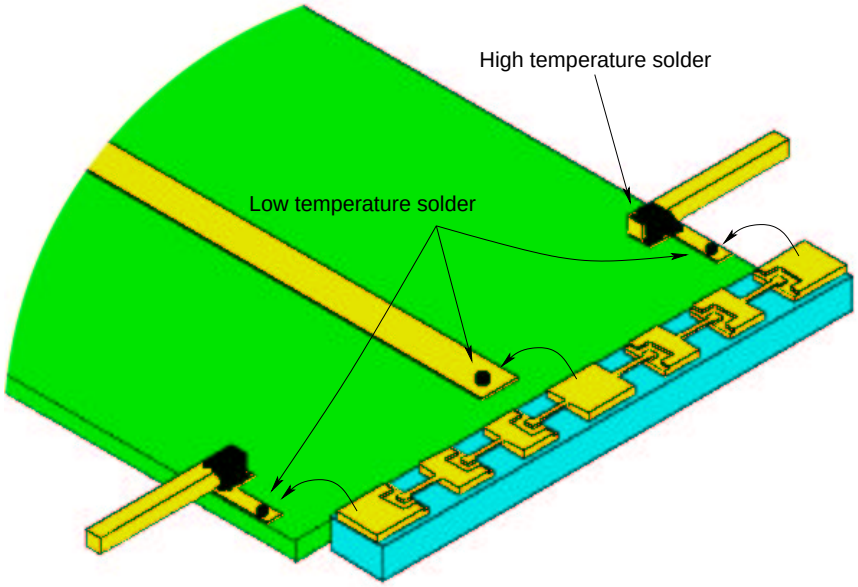


Figure E.2: Close up of the area that receives the diode array. The location of the spots with high and low temperature solder is marked. The diode is also shown placed near the location where it is to be attached.

Next, the metal housing was prepared to receive the assembled quartz circuit. The output back-shorts were constructed into each of the two split pieces by working soft Indium into the appropriate place to plug the reduced height waveguide.

The quartz circuit was placed in the channel in the metal housing and the free ends of the two bond wires next to the diode array were secured to the housing metal surface using small amounts of soft Indium. The DC bias bond wire was soldered to the center pin of the bias connector. DC biasing was verified by the application of reverse and forward biases to the diode array through the bias connector.

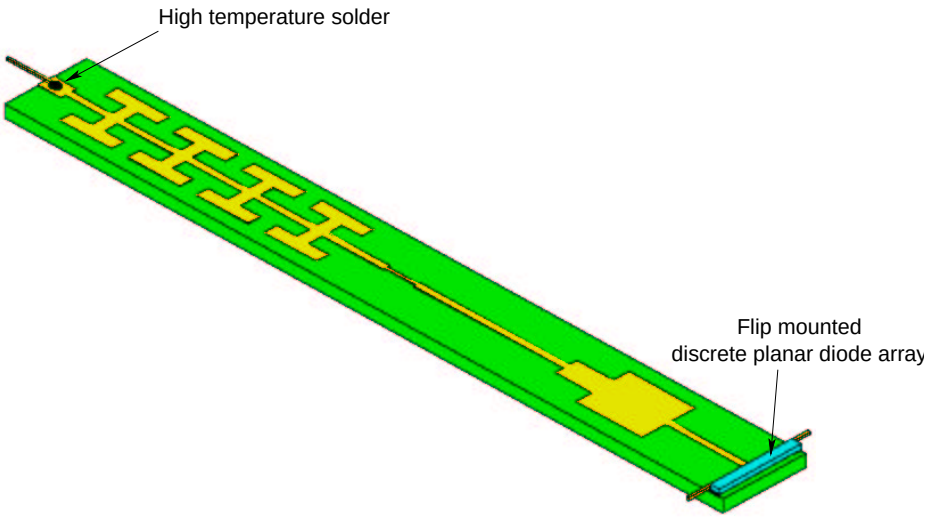


Figure E.3: Diagram of the quartz circuit after completion of the assembly procedure.

Finally the block was closed by placing the other half of the split block on top (guided by dowel-pins) and securing it with screws. The standard waveguide flange adapter sections were then attached to the input and output flanges and the frequency doubler was ready for evaluation.

E.2 Assembly of the 110/220 GHz Frequency Doubler

The process of attaching the discrete planar diode array to the quartz circuit and its subsequent integration into the waveguide block was identical to that for the 55/110 GHz frequency doubler (described in Section-E.1).

E.3 Assembly of the 80/240 GHz Frequency Tripler

The technique of integrating the diode chip and the input and output quartz circuits into the metal housing is described.

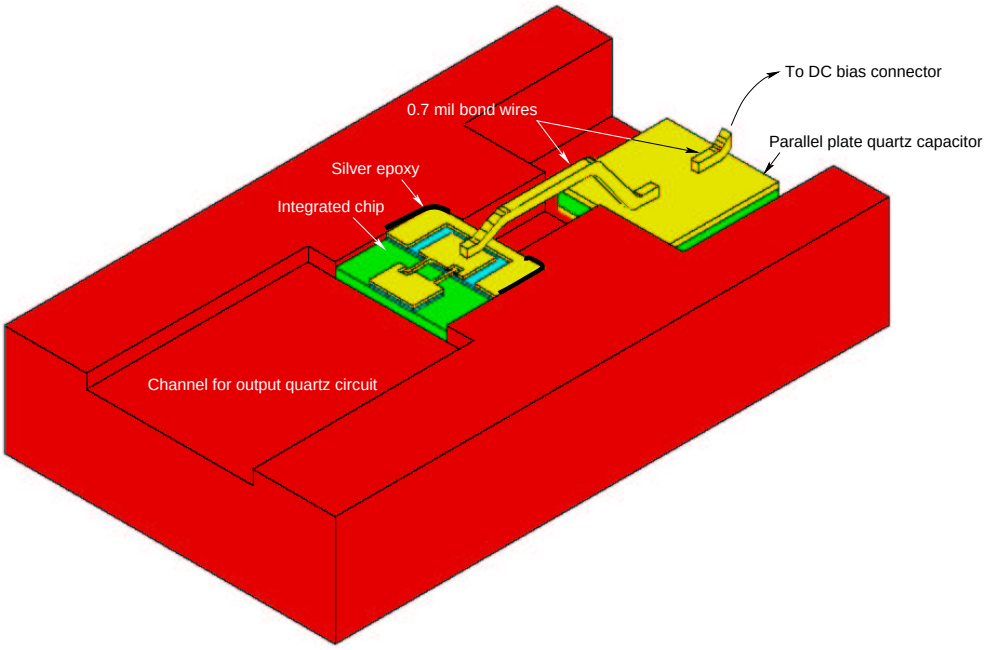


Figure E.4: Cut away view of the metal housing showing the location of the DC bias quartz capacitor and the diode chip. The location of the epoxy used to connect the ground pads to the metal housing is shown. Also shown are the 0.7 mil bond wires used to supply the DC bias to the diode chip.

The first step in assembling the 80/240 GHz frequency tripler was to epoxy the DC bias quartz capacitor and the diode chip into the appropriate locations as shown in Figure-E.4. The epoxy used was a two part silver epoxy, EPO-TEK H20E [155]. As illustrated, the ground pad on the diode chip was also epoxied to the metal housing. The epoxy was cured by placing

the metal block in an oven at 80^oC for 90 minutes. The DC bias pad was then connected to the bias connector by wire-bonding with 0.7 mil wires at appropriate locations as shown in the figure.

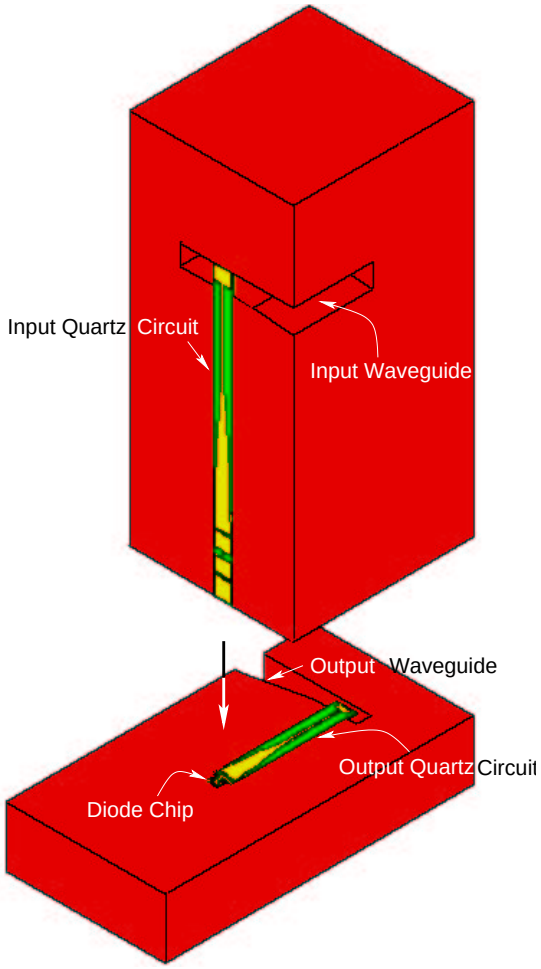


Figure E.5: Cut away view of the relevant pieces of the metal housing showing the relative placement of the diode chip, the input quartz circuit and the output quartz circuit. The DC bias arrangement located adjacent to the diode chip is not shown.

Next, the output circuit was affixed in the channel adjacent to the diode chip using super-glue. The input circuit was housed in the channel located

in the second piece of the metal housing. The relative placement of the diode chip as well as the input and output quartz circuits is shown in Figure-E.5. The connection between the diode chip, the input circuit, and the output circuit was established by carefully applying silver epoxy at the junction and curing the block for 90 minutes at 80^oC in an oven. Figure-E.6 is a photograph of a portion of the metal block that housed the diode chip and the output quartz circuit, prior to the placement of the piece containing the input circuit.

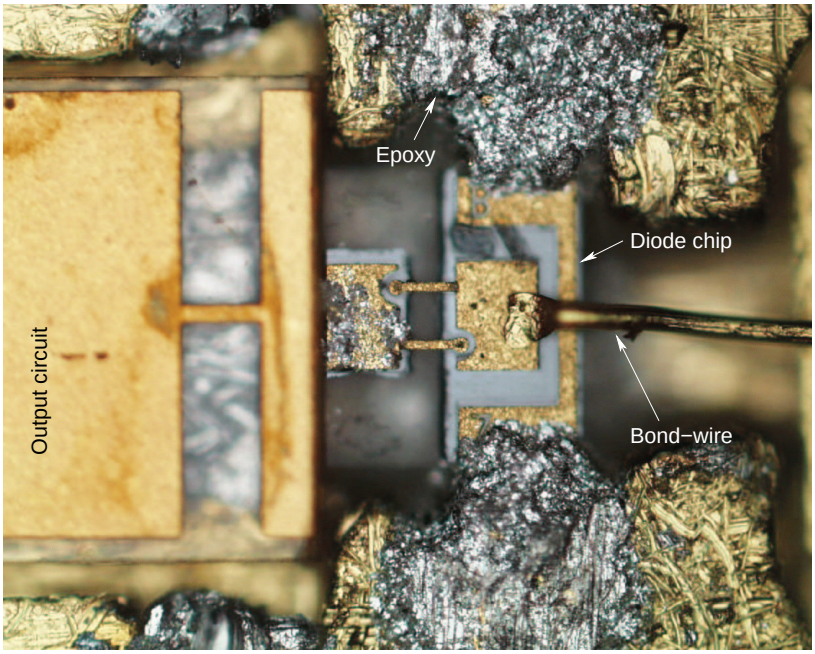


Figure E.6: Photo of the metal block showing the diode chip and the output circuit. A portion of the bond wire used for supplying the DC bias to the chip can be seen. The location of silver epoxy used to ground the chip pads is marked.

The block was then completed by placing the third piece to cover the diode chip as well as the input circuit. The alignment between the three pieces was achieved by strategically placed dowel pins, and held together

with screws. Finally, the standard waveguide flange adapter sections were attached to the input and output flanges and the frequency tripler was ready for evaluation.

E.4 Assembly of the Modified 80/240 GHz Frequency Tripler

The technique of integrating the diode chip and the quartz circuit into the metal housing is described.

The first step in assembling the 80/240 GHz frequency tripler was to epoxy the DC bias quartz capacitor and the diode chip into the appropriate locations. Except for using a modified block, this step was similar to the one illustrated in Figure-E.4 for the previous version of the frequency tripler. As before, the epoxy used was a two part silver epoxy, EPO-TEK H20E [155]. The ground pad on the diode chip was also epoxied to the metal housing. The epoxy was cured by placing the metal block in an oven at 80^oC for 90 minutes. The DC bias pad was then connected to the bias connector by wire-bonding with 0.7 mil wires at appropriate locations as shown in the figure.

Next, the quartz circuit was affixed in the channel adjacent to the diode chip again using silver epoxy, and the block cured at 80^oC for 90 minutes. The connection between the diode chip and the pad on the quartz circuit was established by carefully applying silver epoxy at the junction and curing the block once again for 90 minutes at 80^oC in an oven. Figure-E.7 is a photograph of a portion of the metal block that housed the diode chip and the quartz circuit.

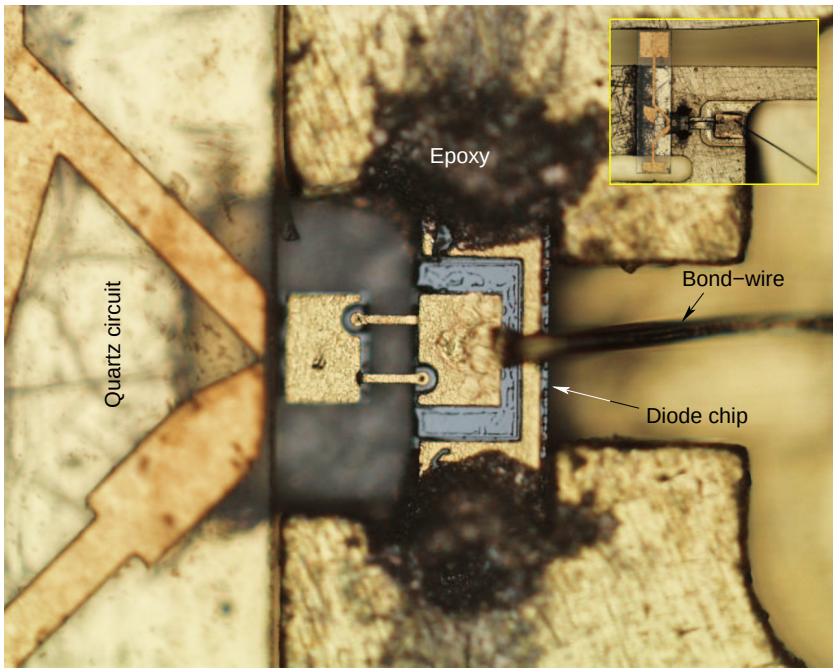


Figure E.7: Photo of the metal block showing the diode chip and the quartz circuit. A portion of the bond wire used for supplying the DC bias to the chip can be seen. The location of silver epoxy used to ground the chip pads is marked. Inset in the top right corner is an overall view of the block showing the entire quartz circuit seated next to the diode chip. The quartz DC bias capacitor as well as the 0.7 mil diameter bond wires can also be seen.

The block was then completed by placing the top half guided by strategically placed pair of dowel pins, and secured tightly into place using screws. Finally, the standard waveguide flange adapter sections were attached to the input and output flanges and the frequency tripler was ready for evaluation.

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Colophon

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