ALMA Memo No. 420

Digital Transmission System Signaling Protocol

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Abstract

The ALMA Digital Transmission System (DTS) transmits digitized IF signals from an antenna to the correlator at the central location. The digitized data is divided equally across four identical transmission elements. Each element formats the parallel data for serial transmission over three 10 Gb/s optical fiber channels and converts it back into parallel data at the receiver. This Virtual Parallel Bus (VPB) system is defined by the channel signaling protocol. The protocol is based upon a 160-bit frame structure using line coding employing scrambling techniques. The frame consists of a synchronization word, a sequence word, payload, and a checksum. Modulo-2 addition of the frame with a pseudo random pattern scrambles the data to provide adequate recovery timing information and a reduction of low frequency content.

1 INTRODUCTION

A signaling protocol for the ALMA Digital Transmission System (DTS) is presented. The DTS transmits the sampled and quantized IF signals from each ALMA antenna to the correlator system at the central location. The digitizer output and the corresponding correlator input is configured as a parallel digital word[1]. Since the data rates are quite high and the correlator system is located some distance from the digitizers, conventional parallel bus systems are impractical. The DTS includes all the digital formatting electronics and electro-optic components required to transmit and receive an antenna's data. The DTS implements the transmission of parallel data with multiple high speed bit serial channels over optical fibers. There are four of these Virtual Parallel Bus (VPB) systems required by each antenna with each VPB employing three separate optical channels.

The VPB performance is determined by the signaling characteristics of a channel. The serial protocol for a single channel describes those characteristics needed for data symbol or bit synchronization, symbol or word identification, and multi-symbol or frame synchronization. For the high data rates, current technology does not provide an economical single optical channel solution. Therefore, the signaling characteristics must also provide for multiple channel synchronization. In addition, the protocol addresses the special electrical characteristics of the physical transmission system. The protocol also defines a system which needs almost no outside intervention.

This memo is organized into nine major sections. The next section supplies a short overview of the ALMA base line plan as it relates to the DTS. Design considerations for a VPB system are described in the following section. The organization of data into frames is next described. The design of the hierarchical synchronization methods for frames and meta-frames follow. The monitoring of data

[1]The term "word" is used throughout to denote a collection of any number of binary bits.

integrity is described followed by the description of channel coding techniques to ensure proper serial channel data reception. The memo ends with a short discussion of suggested self testing capabilities.

The intent of this memo is to specify the signaling protocol of a single optical channel. No attempt is made to described a detailed hardware design. However, the protocol design must be formulated with some consideration of the supporting hardware. Therefore, example block diagrams of representative hardware are used throughout to illustrate principles and design.

2 SYSTEM OVERVIEW

Figure 1 shows a conceptual diagram of the signal data path from an antenna to the center. The receiver front end plan specifies the simultaneous reception of two orthogonally polarized signals. Each receiver polarization can provide an instantaneous bandwidth of 8 GHz which is partitioned into four, 2 GHz wide sub-bands by the IF system. Each sub-band is bandpass sampled at the Nyquist rate and quantized to 3 bits. Thus, one digitizer produces a 12 Gb/s data stream. The digitizers incorporate a demultiplexer which reduces the clocking frequency while increasing the data word size. The baseline plan specifies a 250 MHz clocked 48-bit wide parallel output word. The combined digitized outputs from two orthogonally polarized IF sub-bands produce a 96-bit word at the VPB input. This corresponds to a 24 Gb/s data rate. At each antenna, the DTS will encompass four VPB systems supporting a total data transmission rate of 96 Gb/s.

At the central site, the VPB must supply a 192-bit wide word clocked at 125 MHz to the correlator inputs. A bit position in the received word must correspond exactly to one within a pair of transmitted words. This requires exact synchronization across all optical and electrical components within the VPB. In addition, the VPB must compensate for changes in the propagation times due to variations in environmental factors effecting the optical fibers. With skew and propagation effects eliminated, correct timing sequence is maintained throughout from digitizer to correlator.

Occasionally there are hardware or other system fails. In such a situation when either the digitizer fails or other system elements cause the digitizer to produce incorrect data, the associated VPB should continue to operate properly. This requirement makes the process of quickly and accurately locating the fault possible. In the worst case situation of corrupted data, the input to a VPB would consist of a constant pattern of all zeros or all ones. The serial data stream would then have very few bit transitions resulting in the loss of data and clock recover by the receiver causing the VPB to appear to have failed. Therefore the protocol defines techniques to ensure sufficient channel data transitions independent of the nature of the payload content.

From time to time, there will be service outages, either anticipated or unexpected. In either case, each VPB must be able to restore its exact pre-outage transmission delay without the need for time consuming array calibration involving astronomical observations. This is achieved through a combination of signaling protocol design, hardware design, and some minimal interaction with the array control system.

This section has introduced those system concepts and specifications that drive the design of the DTS. The specifications that each VPB must support are summarized below:

1. 24 Gb/s data transmission rate,
2. 250 MHz transmitter input clock frequency,
3. 96-bit parallel transmitter input data format,
4. 125 MHz receiver output clock frequency,
5. 192-bit parallel receiver output data format,

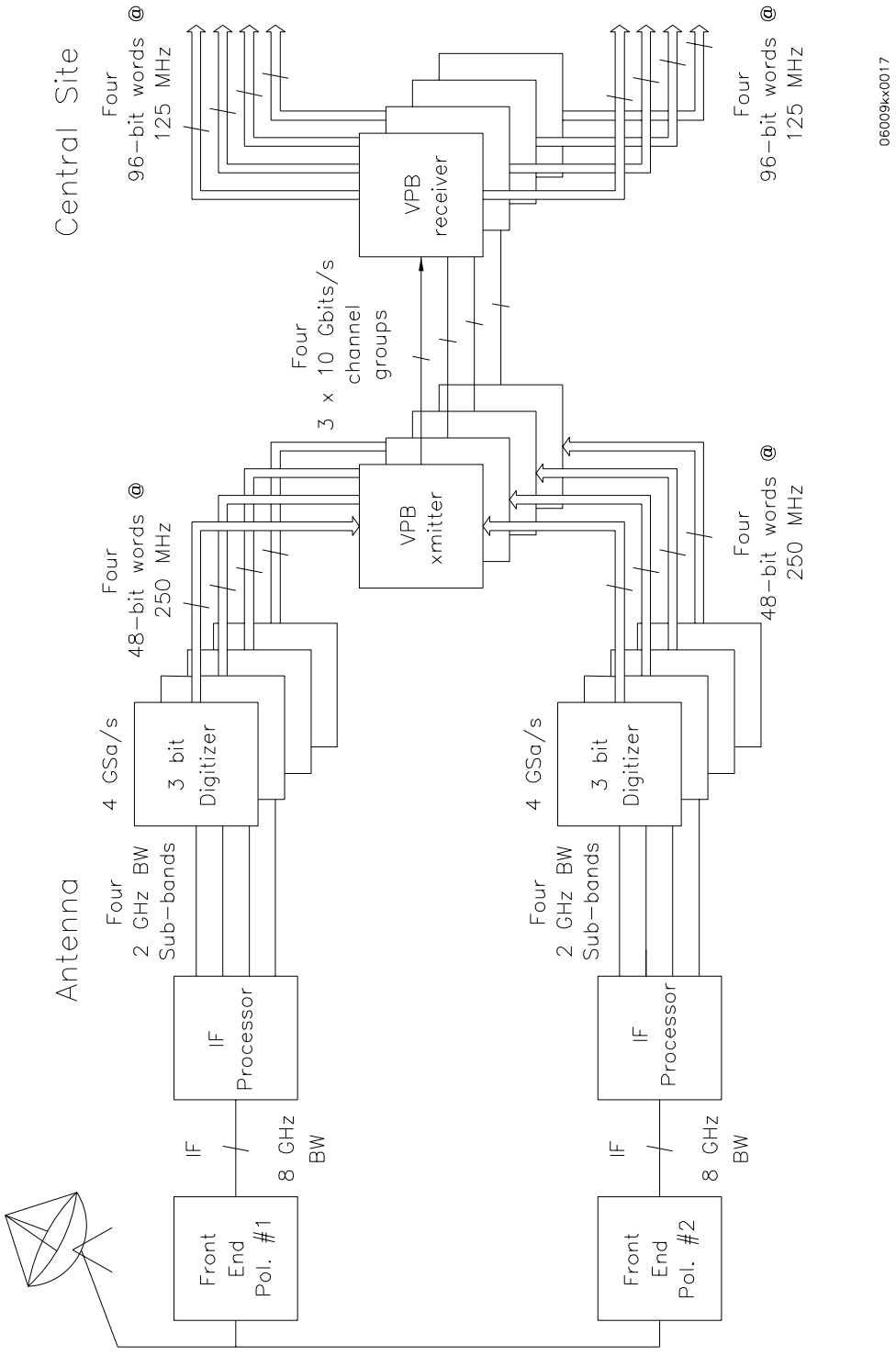

Figure 1: Signal data path from antenna to VPB receiver output.

Number of words	Word size (bits)	Data rate (Gb/s)
2	48	12
3	32	8
4	24	6

Table 1: Three methods of partitioning two digitizer 250 MHz output words.

6. operation over distances of at least 25 Km,
7. deterministic timing after any service interruption,
8. correct operation regardless of payload content,
9. configurable transmission delay,
10. continuous data transmission, and
11. an economical solution and implementation.

3 VPB DESIGN CONSIDERATIONS

The telecommunication industry is driving current technology to supply economical fiber optic components to support high speed signaling standards. One such standard is SONET OC-192. It describes the payload and transport overhead characteristics of an amplitude modulated optical carrier transported on fiber at a signaling rate of 9.95328 Gb/s. This high signaling rate affords ALMA the most economical means to provide high speed optical fiber communication.

For the VPB, the total signaling rate includes not only the payload rate of 24 Gb/s but also some additional supervisory overhead. Therefore, one OC-192 channel does not have sufficient capacity. However, the total payload and supervisory rates can be supported by utilizing multiple synchronized parallel OC-192 channels. The number and size of words which the two digitizer outputs can be partitioned by is shown in Table 1. Also included in Table 1 is the resulting data rate. The smallest number of OC-192 channels which can support the required data rate and some supervisory overhead is three. Thus, the 96-bit VPB input word will be internally split into thirds resulting in three 8 Gb/s data streams. A data rate transformation from 8 Gb/s to 9.95328 Gb/s utilizing a complicated time division demultiplexing and multiplexing scheme is theoretically possible. However, it is impractical due to large clocking ratios and a very large intermediate stage word size (124416 bits clocked at 80 KHz)[2]. But, by increasing the channel clock by less then 0.5% to 10.0 GHz, a much simpler transformation results. In this situation, the input and intermediate rates are identical and a single 40 to 1 multiplexer transforms a 40-bit input word clocked at 250 MHz to a 1-bit word clocked at 10 GHz. The complete VPB is formed from three synchronized modified OC-192 channels operating at this slightly faster rate[3].

This multiplexing leads to a natural grouping or framing of 40 bits. Because the 10 Gb/s channel signaling rate is faster than the 8 Gb/s data rate by 25%, eight additional bits must be added to every

[2]Rate conversion requires determining an intermediate clocking frequency that is an integer divisor of both the input and output clocking frequencies. The input data rate is first reduced by demultiplexing to this intermediated frequency and then increased by multiplexing to produce the output clock. The word size at the intermediate frequency may be larger than either the input or output word sizes by the corresponding frequency ratio. If necessary, fill bits are added or subtracted. An optimum implementation would use an intermediate clocking frequency which is the largest common divisor of both the input and output frequencies. This would require the smallest intermediate word size with the smallest multiplexing and demultiplexing ratios.

[3]Devices from various potential OC-192 IC vendors were investigated for operation at this higher clock rate. The increased clocking was determined not to be an issue.

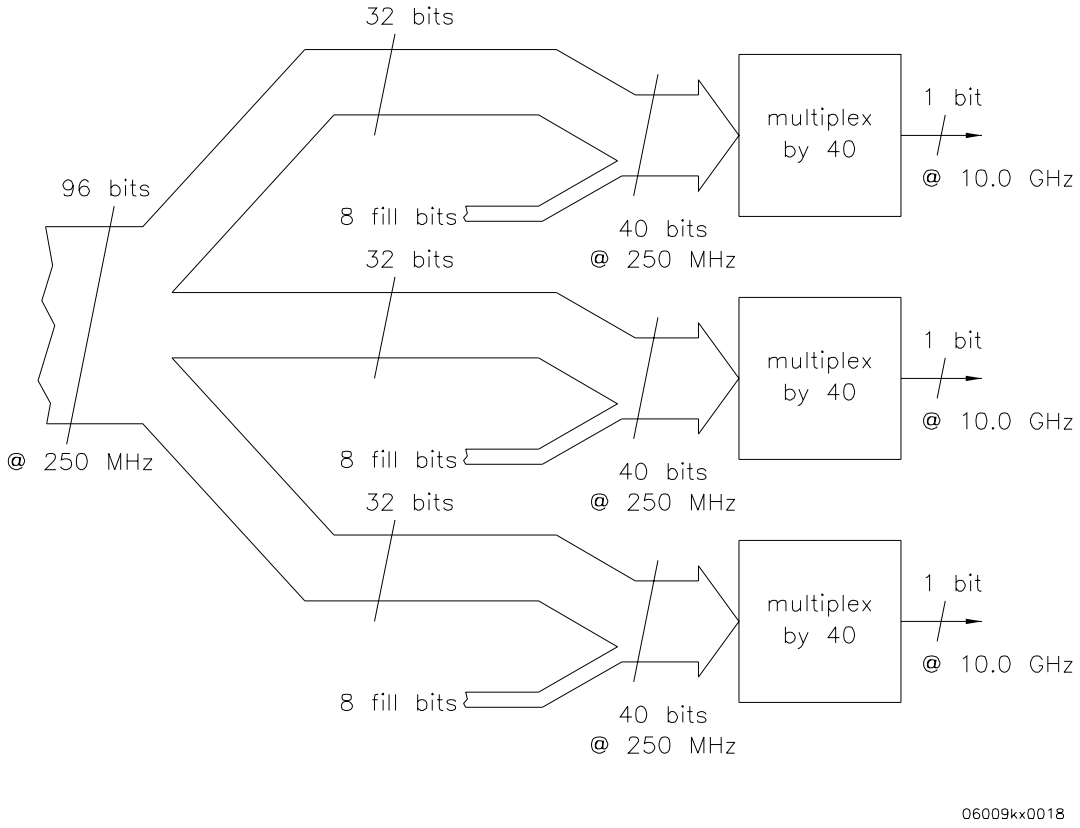

Figure 2: Idealized rate conversion from 96 bits at 250 MHz to 3 1-bit channels at 10 GHz.

32 data bits. Figure 2 shows an idealization of the partitioning of the 96-bit VPB input word, the insertion of three sets of 8 fill bits, and the multiplexing process to produce three 10 Gb/s optical channels.

A benefit of using telecommunication driven technology is the availability of sixteen to one OC-192 speed commodity multiplexer and one to sixteen demultiplexer semiconductor devices. The multiplexer accepts a 16-bit word at 625 MHz and produces a single bit serial data stream at 10 GHz. A data rate conversion can easily be implemented from the VPB input at 250 MHz to the output signaling rate of 10 GHz using a times 2.5 up-rate converter and an OC-192 multiplexer. The receiver performs the inverse operation using an OC-192 demultiplexer and a times 5 down-rate converter to produce an output at 125 MHz. Because of the extra times 2 rate reduction, the received output word is 80 bits wide.

Since the 10 Gb/s channel signaling results from the time division multiplexing of the input word, a mechanism is required to order the received words in the identical bit order as the input. This requires a scheme by which the beginning of a frame can be located in the high speed data stream. A synchronization word is inserted into the fill bits to accomplish this. The receiver searches for and

synchronizes onto this known pattern permitting the reception of the transmitted data in correct order.

With the transmitter input data word spread across three signaling channels, the receiver must be able to de-skew the outputs of the three channels. The VPB must also compensate for changes in propagation delay both across multiple channels and within a single channel. The received data must be delivered with a constant clock independent of externally varying transmission effects. Some of the remaining fill bits of each frame are used for these purposes by creating a large virtual frame or meta-frame from a series of frames. The final ALMA project will contain a large number of VPB systems: a total of 256. Operational issues and reliability will be very important. How will data integrity be verified? What testing capabilities will be used? Additional bits in the frame are used for these purposes. The Bit Error Rate (BER) of the system is expected to be very low[1], less than 10^{-6}, so forward error correction is not necessary. But as the system begins to age, performance will degrade and errors will increase. A checksum over the frame provides advanced warnings of deteriorating performance. It is generated from the transmitted data and inserted into the frame by the transmitter and it is then compared against one generated from the received data. Inconsistencies are then signaled to the ALMA Monitor and Control System.

The signaling protocol is designed to afford a high level of reliability to the ALMA Digital Transmission System. Usually the hardware design determines the system reliability, but there are protocol design features which can improve the system availability or "up" time. With 12 optical channels associated with each one of the 64 antennas, there is a large number of opto-electronic and optical components in ALMA. With 768 high speed optical fiber transmission systems, reliability becomes very important. For example, semiconductor laser devices experience different failure modes, catastrophic failures (the cessation of lazing) and the reduction in signal to noise due to the reduction of optical power with time, and in a wavelength division multiplexing (WDM) system, by a shift in the optical wavelength. Unanticipated failures are very costly in terms of degraded observations. With failures expected, it is essential for the VPB design to maximize the operational diagnostic and monitoring information available. Monitoring of data integrity becomes very important in its ability to identify those channels likely to soon fail permitting maintenance to be planned and scheduled for convenient times.

On a single 10 Gb/s channel, line or channel coding is used to modify the source data stream to facilitate proper reception. Channel coding ensures the transmission of adequate timing information and the minimization of low frequency content [2], [3], [4]. Adequate timing information permits the independence of the source bit sequence and ensures low systematic jitter. Received symbol timing and data recovery is accomplished by a phase locked loop which needs sufficient transitions per reciprocal PLL bandwidth. With more transitions, data is received with less jitter resulting in a lower BER caused by timing errors. With an equal number of ones and zeros, the channel signaling is balanced and contains a small low frequency content. In an AC coupled optical system, this reduces the BER due to the improved stability in detection threshold levels.

Another goal of the DTS design is to minimize the necessity of control from external subsystems. This protocol describes a system which establishes frame and multi-channel synchronization without the use of a reverse channel and independently of all other ALMA systems. To re-establish a prior transmission channel delay or to initialize a VPB system to a specific transmission delay, the ALMA Monitor and Control (M&C) system interfaces with only the VPB receivers at the central site. The M&C system monitors various operational VPB parameters, but is not involved in controlling normal routine operations.

The last consideration is cost. With the construction of a large number of systems, the unit cost is important. One way to minimize cost is to use commercially available products wherever possible. The hardware implementation of this protocol is supported by commercial optical and semiconductor products designed for the SONET OC-192 market.

This section has introduced the issues, concepts and design considerations of the VPB system. The

design considerations are summarized below.

- Three rate modified OC-192 channels operating at a signaling frequency of 10 Gb/s are used to transmit the payload.
- Data rate conversion exploiting time division multiplexers transforms a 32-bit word at an input frequency of 250 MHz to a 1-bit serial data stream at 10 GHz.
- At reception, a rate conversion transforms the 10 GHz 1-bit serial data stream to a 64-bit word clocked at 125 MHz.
- The insertion of fill bits increases the input word size by 25% to accommodate the faster signaling rate.
- Multiple bits are collected into frames.
- The received data is correctly timed by the use of frames and meta-frames.
- High operational reliability is achieved by design and by continuously monitor the data for errors.
- The implementation is cost effective.

The VPB signaling protocol design decisions have also been introduced and are summarized below.

- A framing or synchronization word facilitates frame extraction after time division demultiplexing.
- The use of a meta-frame facilitates multi-channel synchronization and the elimination of propagation effects.
- A checksum word continuously monitors data integrity.
- Data scrambling is used to minimize bit sequence effects, low frequency content, and to maintain a balanced signal.

These issues and the frame size and its organization are discussed in the sections which follow.

4 FRAME IMPLEMENTATION

At the transmitter, the 250 MHz to 10 GHz rate conversion produces a natural frame size of 40 bits. At the receiver, there is a 10 GHz to 125 MHz rate conversion. This produces a natural frame size of 80 bits. However, even this frame with its large excess channel capacity of 25% does not have enough extra bits to contain all the necessary supervisory information. This information consists of a synchronization pattern, the meta-frame and multi-channel synchronization words, and the data integrity checksum. Thus, a frame with a larger supervisory bit capacity is needed. Any frame size which is a multiple of 80 bits is suitable. To provide sufficient supervisory capacity, a frame size of 160 bits is chosen. This choice provides 32 bits for supervisory information, while still maintaining a small frame size and accompanying low implementation cost.

At the transmitter, four consecutive 32 bit input words are demultiplexed to produce one 128-bit data word. As shown in Figure 3, 32 additional bits are added to this 128-bit data word to produce a 160-bit frame. The frame rate frequency is 62.5 MHz. The frame is then time division multiplexed by 160 to produce the 10 Gb/s output bit stream. As a practical matter, two 80-bit words, each derived from separate halves of the frame word, follow different data paths through two 5 to 1 multiplexers

to an output selector switch. This selector logic switches on opposite phases of a 312.5 MHz clock producing a sequence of 16-bit words clocked at 625 MHz. This approach is necessary to overcome speed limitations in the logic hardware (a field programmable gate array device) most likely used to implement the data formatter.

A partitioning and re-ordering circuit is required in the data path to achieve the identical bit ordering at the transmitter's serial output bit stream as in the internal 160-bit frame word register. The partitioning circuit operates on 16 bit words and is placed between the data combiner and the two 5 to 1 multiplexers. This re-ordering is necessary to correct for the 16-bit word shuffling introduced by the output selector switch. The output of the selector switch drives the high-speed 16 to 1 multiplexer which generates the final 1-bit 10 GHz data stream. A simplified transmitter block diagram showing the 32-bit input bus, the input rate converter, the data combiner, the partition and re-ordering circuit, the two times 5 multiplexers, the output selector switch and the final times 16 multiplexer is presented in Figure 3. The 32 supervisory bits associated with every 128 data bits are used for frame and meta-frame synchronization and the transmission of the checksum word.

The mapping of serialized frame bit locations to internal data registers, an input or output word, the synchronization pattern word, the meta-frame sequence word or the checksum word, is completely arbitrary. The frame's organization defines a bit's function and thus determines its location within the registers of the transmitter and receiver formatter. Serial bit transmission begins with bit 0[4] of the internal 160-bit register word. One channel clock period later (100 ps), bit 1 is transmitted. This continues in sequence until all 160 bits have been transmitted. De-serialization is done in reverse, the first received bit becomes bit 0 of the 160-bit received word and so on.

Each frame contains 128 bits of payload and 32 bits of supervisory information. The supervisory information is composed of a 10-bit synchronization pattern, a 5-bit sequence count, a single meta-frame index bit, and a 16-bit checksum. The payload contains four successive 32-bit transmitter input words ordered by arrival. The following three sections describe these components in detail.

Six of the 10 synchronization pattern bits start the frame at location 0. They are followed by the single meta-frame index bit at location 6. The 5-bit sequence count follows. The remaining 4 bits of the first 16 frame bits contain the first portion of the payload. The remaining 4 bits of the synchronization pattern begin at the start of the next 16 bits, location 16. Separating the 10-bit synchronization pattern across two 16-bit frame sequences is necessary for frame synchronization due to an ambiguity introduce at the receiver by the same type of 16-bit word shuffling as produced by the transmitter selector switch. Continuing at location 20 are the remaining 124 bits of the payload. The last 16 bits of the frame holds the checksum value. Bit 0 of the first 32-bit transmitter input word maps to frame bit 12 and bit 31 of the fourth 32-bit transmitter input data word maps to frame bit 143. The frame organization is presented in Figure 4.

5 FRAME SYNCHRONIZATION

A simplified data path block diagram of the DTS receiver de-formatter is shown in figure 5. It contains a data selector switch located between the high-speed 1 to 16 demultiplexer of the Clock and Data Recovery (CDR) device and the two 1 to 5 demultiplexers. This selector switch permits the demultiplexer pair to operate at one-half the output rate of the CDR device.

Similar to the situation with the transmitter, the receiver selector switch shuffles the order of arriving data. Alternating blocks of 16 bits follow two different signal paths. Each path contains a 1 to 5 demultiplexer. These two demultiplexers operate in synchronism to produce two 80-bit words at

[4]The numerical value of a bit designation does not imply any real value or meaning. It is an arbitrary enumeration intended solely to identify the bit within a data word.

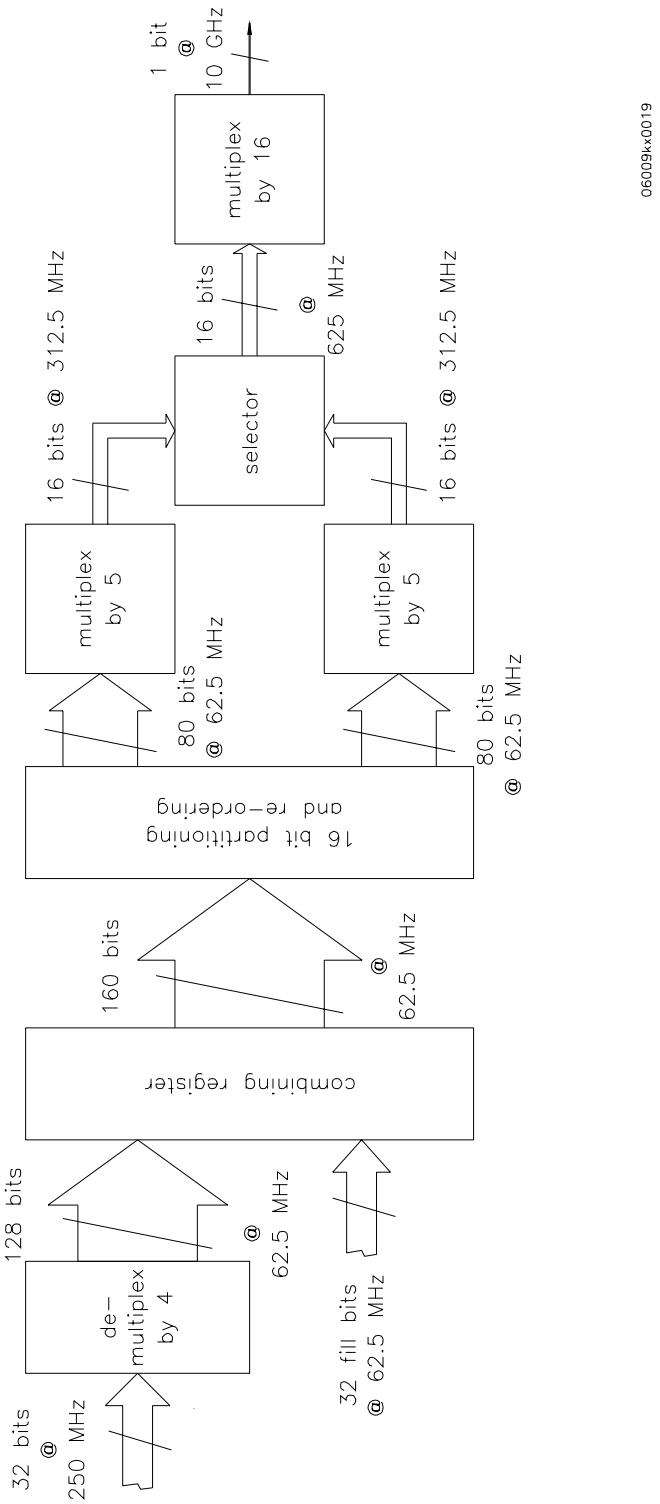

Figure 3: Production of the 10 Gb/s serial data stream from four consecutive 32-bit input data words, two 16-bit fill words, a 16-bit word re-organizer, two 5 to 1 multiplexers, one 16-bit word selector switch, and one 16 to 1 high-speed multiplexer.

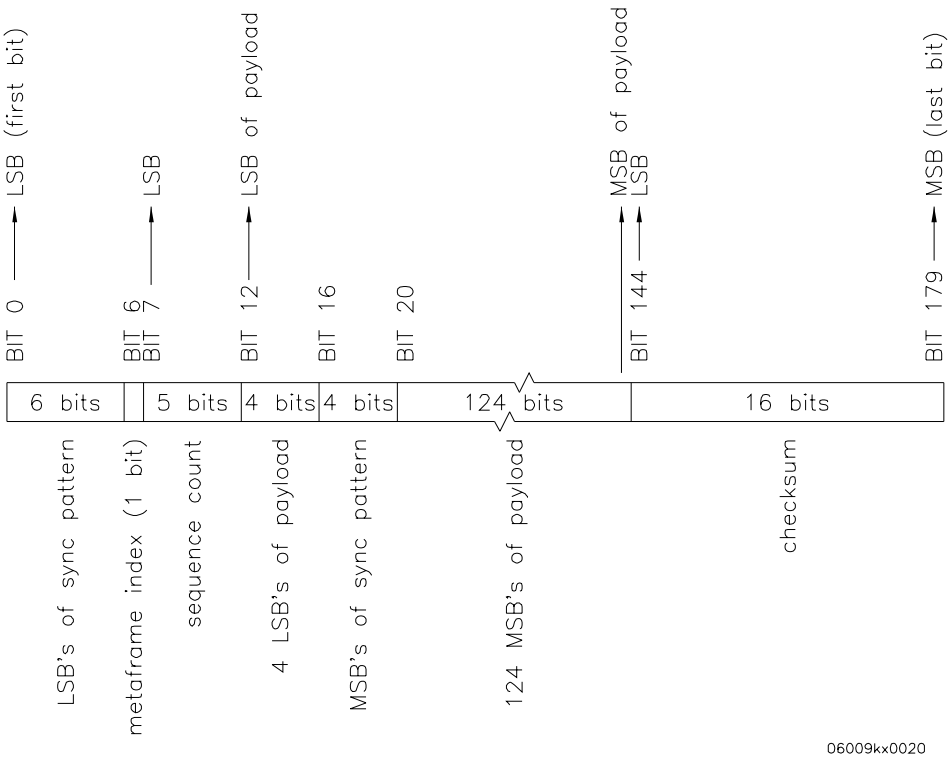

Figure 4: 160-bit frame organization.

62.5 MHz. These two words are connected to the input of a configurable re-ordering and combining circuit which compensates for the shuffling action of the data selector switch. The result is a 160-bit output word which should replicate the bit order of the received data stream.

The order of alternating 16 bit data blocks is determined by the initial state of the data selector. If this state is incorrect, the block sequence is reversed and it does not match the received data. To correct the sequence, the re-ordering circuit exchanges the input data from the two paths. By partitioning the synchronization word across two 16-bit frame words, it is possible for the receiver to determine the initial state of the data selector and to correctly un-shuffle the resulting data to replicate the received bit stream.

The 10-bit synchronization pattern is a unique sequence of bits and is always placed at the some location within each frame The first bit of the synchronization pattern corresponds to the bit 0 of the 160-bit frame. The synchronization pattern must be long enough and have special characteristics to provide a means to unambiguously locate the start of each frame. Suitable patterns have been studied by researchers [5], [6], [7], and [8]. The chosen pattern must also be larger than the length of the shift register generator which produces the scrambling pattern. If not, the synchronization pattern could be detected within the scrambling pattern incorrectly locating the frame. The chosen pattern is binary 1001010110. Its bit order is unimportant so its bit sequence could be reversed.

Frame synchronization progresses through three stages at the receiver: the search stage, the check stage and the monitoring stage. A candidate frame is randomly selected from 160 consecutive bits of the incoming serial bit stream. The ten bits containing the potential synchronization pattern are checked for the presence of that pattern. If unsuccessful, another candidate frame is selected and the comparison repeated. The second frame immediately follows the first frame but after a delay. The search process begins with a delay of one channel bit time. After each unsuccessful comparison, this delay is increased by one bit time. The process of delay incrementing and pattern comparison repeats until a match is found. If no match is found after 160 comparisons, the data shuffler and combiner circuit is configured to select the alternate data organization and candidate frames are searched using the same algorithm. The pattern matching criterion requires that all ten synchronization pattern bits match.

Once a potential frame is located, the synchronization process enters the second or check stage. With a pattern of only ten bits in length, the probability of correctly detecting the synchronization pattern in a data stream with equally likely occurrences of ones and zeros is 99.90%. Even though this probability is less than one false detection per frame, the detection accuracy can be increased. The check stage performs this task. At least six of the subsequent seven frame synchronization patterns must also successfully match to verify that the true frame has been located. This approach allows for the possibility of one transmission bit error in 8 frame synchronization words. If the check procedure fails, the system returns to the search phase and begins a new search. To optimize this search, the first selected frame is chosen from the current bit stream location delayed by one channel bit time. After successfully locating the synchronization pattern, the probability that it is a false location is $8.47 * 10^{-22}$ or about one frame in 37 centuries.

In the monitoring stage, the system continually monitors the synchronization pattern for frame slippage. Two sequential mismatched frames or the mismatch of more than one in eight sequential frames will return the system to the search stage. As in the check phase, the search begins as soon as an error has been detected from the current bit stream location delayed by one channel bit time.

6 META-FRAME IMPLEMENTATION

A synchronization method is required to maintain frame concurrence across the three optical channels of the VPB. If the transmitter simultaneously inserts an identical incrementing count into each channel's frame, the receiver has a method by which it can maintain synchronization across all channels. This

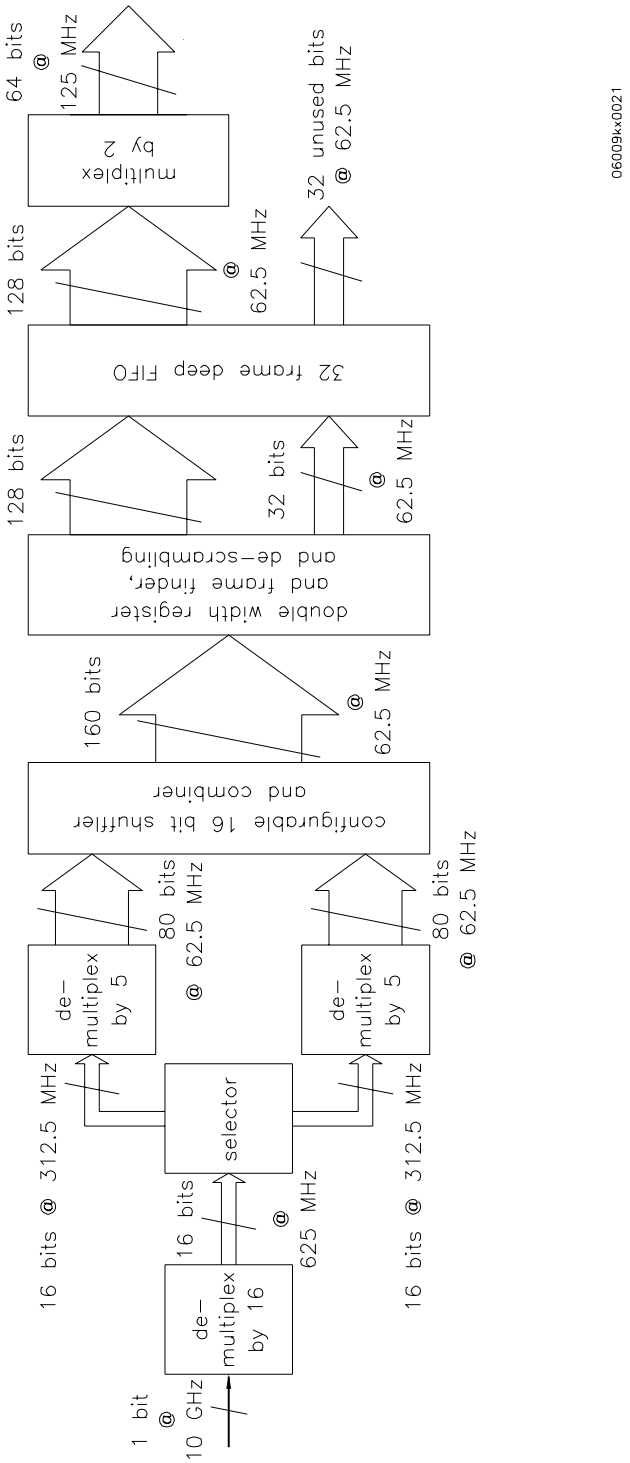

Figure 5: A simplified data path block diagram of the receiver formatter showing the high-speed 1 to 16 demultiplexer, the data selector switch, two synchronized 1 to 5 demultiplexers, the configurable 16-bit word shuffler and combiner, a block containing the frame finder and de-scrambler, and the 32-frame deep FIFO and the 2 to 1 output multiplexer.

Fiber Type	D(@ 1530 nm)	D(@ 1565 nm)	Delay
Standard	15.8 ps/nm/Km	17.8 ps/nm/Km	14.7 ns
LEAF	2 ps/nm/Km	6 ps/nm/Km	3.5 ns

Table 2: Dispersion values and maximum dispersive signal delay for 25 Km lengths of two different fiber types

count is extracted by the three receivers, compared, and frame delays applied to the early arriving channels. The result will be three simultaneously clocked 160-bit frames with the identical incrementing count. Therefore, the 192-bit word produced by the receiver will be identical to two consecutively transmitted 96-bit words.

Together with the unique synchronization pattern, the full range of sequence numbers effectively creates a large virtual frame or meta-frame. The size (duration in time) of the meta-frame must be at least as great as the largest expected propagation time differences between channels. Inter-channel propagation differences arise because of inherent differences in fiber characteristics and variations in dispersion and group delay with environment. Representative dispersion values for large effective area single mode optical fiber (LEAF) optimized for use in wavelength division multiplexing (WDM) applications in the conventional band (C band: 1530 nm to 1565 nm) are 2 ps/nm/km to 6 ps/nm/km[9]. Other single mode fiber types have dispersion values ranging from about 16 ps/nm/km to 18 ps/nm/km[10]. For 25 km of LEAF fiber and assuming a worst case situation of two optical carriers separated by the maximum wavelength of 35 nm, the propagation difference amounts to 3.5 ns or 35 bits. For standard single mode fiber, the maximum delay is 14.7 ns or 147 bits. Table 2 summarizes this information. These values scale linearly with distance. For the planned distances and fiber types, a meta-frame consisting of at least two 160-bit frames should be satisfactory.

Individual counters associated with each optical channel, all synchronized to a common external event, are used to generate the sequence number. Any external event could synchronize the counters. Currently there is no requirement to reference the meta-frame to any event. But since there is a 20.833 Hz phase stabilized clock at both the central site and at each antenna, it could be easily used as a suitable event. To uniquely count each frame within the 48.000 ms period (20.833 Hz clock) requires 22 bits, an amount not readily available. Since the meta-frame size is somewhat arbitrary, but it should evenly divide the 48 ms period, a size of 32 frames is chosen. This meta-frame sequence count begins at frame bit 7. These meta-frames are sufficient to uniquely identify frames from separate channels with propagation delay differences up to approximately 100 meters.

A 5-bit word holds the repeating meta-frame sequence value. The word counts from 0 to 31 and is then reset to 0. The 20.833 Hz clock is used as the external event to synchronize the counters for the three data channels. One additional bit[5] is used to indicate the first meta-frame following the external event. This marking facilitates measuring a channel's transmission delay to the nearest frame or 16 ns.

Data transmission length compensation is achieved as a simple by-product of meta-frame synchronization. The probable hardware implementation involves a first-in first-out (FIFO) register. This design allows the receiver to easily select frames with arbitrary delays. Any prescribed delay within the size range of the FIFO can be specified by the M&C system. Cable dispersion effects require a FIFO size of at least three frame times (48 ns). Total array fiber length compensation is achieved simply when the FIFO is made large enough. For the baseline ALMA array, the longest anticipated fiber runs are 25 Km. Levine [11] has measured the temperature coefficient of various optical fibers. Using a representative value for jacketed Siecor optical fiber of 25 ppm per degree Celsius, the maximum length change for a temperature change of 50C corresponds to about 150 ns. The FIFO depth is twice this size

[5]See bit 6 in Figure 4.

(system initialization could occur at either the shortest or the longest fiber length) and is no greater than the meta-frame. Therefore, a 32 frame deep FIFO compensates for the worst case of line length changes.

The incorporation of the meta-frame index permits a receiver to count the number of received frames between its external event and the arrival of the index. Multiplying this value by the frame duration and adding to the FIFO delay value provides the total transmission delay. The M&C system can read and archive the total transmission delay for any antenna.

7 DATA INTEGRITY

The intrinsic bit error rate of the electro-optical components in the fiber transmission system is expected to be extremely low[1]. However, in addition to the laser diode source, high speed modulator, photodiode detector, AGC amplifier, and the clock and data recovery electronics associated with each channel, the ALMA system includes a large reconfigurable network of optical fiber and connectors. With a large number of individual channels comprising complex high speed components combined with multiple fiber segments and interconnections all organized into a complex system, a continuously operating automatic performance monitoring method is essential. To be useful, such a system must be operationally simple and robust. The last 16 bits of each frame are used to hold a checksum of the previous 144 bits.

Commonly used error checking methods include algebraic checksums, parity checks, longitudinal parity and redundancy codes, and cyclic redundancy codes (CRC). A simple procedure produces a longitudinal parity check word by the modulo-2 addition of the first nine 16-bit words within the frame. This method detects all odd numbers of errors introduced throughout the entire transmission system. A more robust method would use a CRC method where the 144 frame bits are modulo-2 divided by a 16-bit generator polynomial. The resulting 16-bit remainder provides the checksum value. The CRC method is more complex than is required and is replaced by the computationally simple longitudinal parity.

8 SCRAMBLING

Channel coding is the process of modifying the source data stream to facilitate proper reception. The data source is composed of payload information, whose characteristics are known only in a statistical sense, and supervisory information. The characteristics of the synchronization pattern and meta-frame sequence count of the supervisory information are also known, but not those of the 16-bit checksum word. Channel coding is essential in providing adequate data transitions for proper bit synchronization and in reducing low frequency content regardless of the source's characteristics [12]. The coding mechanism must, therefore, satisfy these two requirements.

Scrambling is a classical technique which achieves both of these requirements [13]. Numerous scrambling techniques and their synchronization methods have been described in the literature [4], [14], [15], [16]. The frame synchronous scrambling (FSS) method used in the synchronous digital hierarchy (SDH) is used. With the exception of the 10-bits comprising the synchronization pattern, all bits in the frame are scrambled by a frame static random pattern. This permits easy frame detection by locating the unaltered synchronization pattern. The scrambling pattern is added modulo 2 to 150 bits of the frame with the first scrambling pattern bit added to frame bit 7.

The scrambling pattern is produced by a maximal length shift register generator (SRG) with a period less than the frame length. The pattern "runs" continuously throughout the entire 150 bits of the frame. A seven stage SRG producing a 127-bit length sequence is used. The 150-bit pattern produced with a generator polynomial of $1 + x^6 + x^7$ and a seed or initial value of hexadecimal 64 has

run length	number of ones	number of zeros
1	20	19
2	10	11
3	5	5
4	2	2
5	1	1
6	0	1
7	1	0

Table 3: Run length distribution of ones and zeros for the 150-bit scramble pattern.

the randomness properties proposed by Golomb [17]. The scrambling pattern has 75 ones and 75 zeros achieving perfect DC balance. Table 3 shows the run length distribution of ones and zeros.

Table 3 also indicates the small amount of low frequency content in the pattern. The scrambling pattern has only 4 runs of length greater than 4 bits with the longest one being 7 bits. With a frame static pattern, the scrambling operation is performed in parallel across all frame bits from a single pre-loaded 160-bit long register. This register is implemented as an array of 20 byte-sized words which are loaded with the desired pattern.

9 SELF TEST METHODS

With ALMA containing a large number of these complex high speed systems, self testing mechanisms are essential. These capabilities are different from the error monitoring afforded by the inclusion of the checksum. Once a system fault has been detected, procedures are necessary to enable maintenance personnel to quickly isolate and repair the fault. Even though these methods and procedures are not strictly part of the signaling protocol, a short discussion is necessary in guiding the design of the frame generation and reception hardware.

To check the clock recovery circuitry, a simple alternating pattern of ones and zeros is transmitted. In this mode, there is no frame or meta-frame synchronization, checksum calculation, nor scrambling operation performed. Replacing 10 bits of alternating ones and zeros with the synchronization pattern, enables frame detection diagnostics. Enabling the 5-bit incrementing sequence number provides multiple channel synchronization testing. Scrambling is tested by enabling the scrambler with fixed payloads of all zeros or all ones. In both previous cases, the checksum generation is disabled. The final diagnostics evaluate the checksum system. One test involves generating a checksum over 144 bits containing a 134-bit scrambled pattern of zeros plus the unscrambled 10-bit synchronization pattern. Another test, replaces the 134 scrambled zero bits with scrambled ones. The remaining tests involve forcing an error in the checksum generation using the previous simple payload patterns. Table 4 summarizes these diagnostics.

Most of these diagnostic tests benefit from an implementation which utilizes a 20 byte dynamically loadable scrambling register. By combining the ability to disable the input and changing the scrambling pattern, all tests except those involving checksum generation are possible.

10 CONCLUSION

A signaling protocol has been described for the serial channels of the Virtual Parallel Bus system of the ALMA Digital Transmission System. It is based upon a structure of 160 bits organized into a frame. The frame configuration contains a synchronization pattern, a sequence word, an index bit, 128 bits

10 GHz clock recovery	160 bits of alternating ones and zeros
frame detection	sync. pattern + 150 bits of alt. ones and zeros
multiple channel synchronization	sequence word + 145 bits of alt. ones and zeros
scramble + data pattern #1	enable scrambler plus 145 bits of zeros
scramble + data pattern #2	enable scrambler plus 145 bits of ones
checksum with pattern #1	checksum of 128 + 5 + 1 bits of zeros + sync. pattern
checksum with pattern #2	checksum of 128 + 5 + 1 bits of ones + sync. pattern
forced checksum error #1	erroneous checksum for 128 + 5 + 1 bits of zeros
forced checksum error #2	erroneous checksum for 128 + 5 + 1 bits of ones

Table 4: Minimum suggested diagnostic modes.

of payload, and a checksum. Frame synchronization is achieved with a 10-bit pattern located at a known location within the frame. Cross channel synchronization is obtained by inserting the identical incrementing 5-bit value cycling through 32 discrete values into the three channels of the VPB. To monitor system performance, a 16-bit checksum value is inserted into the frame. In addition, a method of line coding has been described which provides timing information and reduces low frequency content. Scrambling the frame data by the modulo-2 addition with a random pattern achieves these desired results. These characteristics define a VPB system which transmits 24 Gb/s from one parallel interface to another operating as a stand alone system independently of all other ALMA systems.

11 ACKNOWLEDGMENT

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